

"A MEMORY DEVICE"

This invention relates to a semiconductor memory
5 device, and more particularly to a technology which
is effective when applied to a static RAM of large capacity.

As stated in 'Nikkei Electronics' issued on September
26, 1983, pp. 125 - 139, static RAMs have increasingly
been enlarged in capacity and enhanced in speed. First,
10 the arrangement of a static RAM will now be briefly
explained.

Fig. 1 of the accompanying drawings shows an example
of the whole arrangement of a semiconductor memory device
which we have previously developed.

15 The memory device 100 shown in Fig. 1 has a
memory mat 10 in which a large number of memory cells
M are arrayed in the shape of a matrix consisting of
rows and columns, an X decoder/driver 20 and a Y decoder
30 which serve to select the memory cell within the
20 memory mat 10 on the basis of address data A_i , and so
forth.

The X decoder/driver 20 decodes the lower (or upper)
bit data of the address data A_i , to prepare alternative
select signals $X_0 - X_m$. The select signals $X_0 - X_m$
25 are applied to word lines W which are laid in the row

direction of the memory mat 10.

The Y decoder 30 decodes the upper (or lower) bit data of the address data A_i , to prepare alternative select signals $Y_0 - Y_n$. The select signals $Y_0 - Y_n$ are applied to a Y select switch bank (column switch bank) 40. The Y select switch bank 40 operates to select any of complementary data line pairs D and $\bar{D}$, each pair of complementary data lines being laid in the column direction of the memory mat 10.

In the above way, the memory cells M within the memory mat 10 are respectively selected in the row direction and the column direction. The memory cell M , which is connected in the place of intersection between the row and the column selected on the basis of the address data A_i , is connected to common data lines $L1$ and $L2$ through the selected complementary data line pair D and $\bar{D}$ as well as the Y select switch bank 40. The change of potentials appearing on the common data lines $L1$ and $L2$ is detected by a read sense circuit 50, and the detected result becomes the read output D_{out} of stored data.

Fig. 2 of the accompanying drawings shows part of the internal circuitry of the memory device illustrated in Fig. 1, which part we have previously developed.

As shown in Fig. 2, each of the paired complementary

data lines D and $\bar{D}$ has one end thereof connected to a common power source V_{cc} through a MOS field effect transistor for pull-up m11 and has the other end thereof connected to the common data line $L1$ or $L2$ through a
5 Y select switch (column switch) $s1$ or $s2$ included in the Y switch bank 40. Accordingly, the stored information written in the selected memory cell M can be read out in such a way that the change of the potentials complementarily appearing on the common data lines $L1$ and $L2$ is detected
10 by the read sense circuit 50. The select switches $s1$ and $s2$ in the Y select switch bank 40 are respectively constructed using MOS field effect transistors.

The Y select switches $s1$ and $s2$ are all rendered OFF (non-conductive) in a non-selected mode, that is,
15 when no valid address data are input. At this time, the common data lines $L1$ and $L2$ are connected to none of the complementary data line pairs $D, \bar{D}$. On this occasion, there arises the condition that the common data lines $L1$ and $L2$ fall into floating states and that
20 their potentials are not fixed.

When the common data lines $L1$ and $L2$ have become the floating states in the non-selected mode, charges having been stored in capacitors parasitic thereto are discharged meantime, and the potentials of these common
25 data lines $L1$ and $L2$ lower down to considerably low

potentials (for example, potentials close to the ground potential). Therefore, when any memory cell is subsequently selected to read out information stored therein, a long time is taken before the potentials of the common data lines rise up to those at which the sense circuit for detecting the potential change of the complementary data line pair operates stably, and a long access time is involved.

We have therefore attempted to design the circuit, as illustrated in Fig. 2, such that a bias circuit 60 is utilized and the common data lines L1 and L2 are always supplied with fixed potentials (potentials close to those at which the sense circuit operates stably), thereby to shorten the access time.

The bias circuit 60 devised by us as shown in Fig. 2 is such that impedance elements Z1, Z2, Z3 and Z4 formed of MOS field effect transistors are employed for assembling two sets of voltage divider circuits (Z1 and Z3, and Z2 and Z4), and that voltages at respective voltage division points are applied to the common data lines L1 and L2. The two sets of voltage divider circuits (Z1 and Z3, and Z2 and Z4) are respectively connected across the common power source V_{cc} and the ground potential, and they supply the corresponding common data lines L1 and L2 with the voltages obtained

through the resistance voltage division of the voltage across the common power source V_{cc} and earth potential. Thus, the common data lines L1 and L2 are avoided from falling into the electrically floating states and are
5 biased at fixed potentials. The MOS field effect transistors as the impedance elements Z1 - Z4 are respectively controlled to turn ON so as to have predetermined equivalent resistances (impedances) by fixed control voltages V_{s1} and V_{s2} .

Meanwhile, we have carried out research from the
10 viewpoints of lowering the power consumption and enhancing the operating speed of a static RAM and have developed a technology wherein a static RAM is constructed using both bipolar transistors and MOS transistors. The outline of the technology is as stated below. In an address circuit,
15 a timing circuit etc. within a semiconductor memory, an output transistor for charging and discharging a signal line of long distance and an output transistor of large fan-out are formed of bipolar transistors, while logic circuits for executing logic processes, for example,
20 the processes of inversion, non-inversion, NAND and NOR are formed of CMOS circuits. The logic circuit formed of the CMOS circuit is of low power consumption, and the output signal of this logic circuit is transmitted to the signal line of long distance through the bipolar
25 output transistor of low output impedance. Since the

output signal is delivered to the signal line by the use of the bipolar output transistor having the low output impedance, the dependence of a signal propagation delay time upon the stray capacitance of the signal

5 line can be lessened, this function realizing the semiconductor memory of low power consumption and high speed.

On the basis of the above technology of the high speed and low power consumption SRAM employing the bipolar-CMOS hybrid technology, we have further studied
10 the enhancement of an access time. As a result, it has been revealed better for shortening the access time to lower the potential of a common data line and to render the impedance of the common data line (or the amplitude of a signal on the common data line) smaller.

15 That is, it has been found that when the impedances of the common data lines L1 and L2 are rendered as small as possible, time constants which are determined by capacitances C_{s1} and C_{s2} parasitic to the respective common data lines L1 and L2 and the impedances of these
20 common data lines can be reduced, so the signal transfer speeds of the common data lines can be enhanced.

It has also been found that when the potentials of the common data lines are high, a differential pair of transistors Q1 and Q2 constituting the sense amplifier
25 SA 50 as shown in Fig. 2 come to have high base potentials

and become close to saturation because of constant collector voltages, so this forms one factor of lowering the signal transfer speeds.

When it is intended as a countermeasure to reduce
5 the impedances of the common data lines and to lower the potentials thereof by the use of the common data line potential generating circuit 60 shown in Fig. 2, the ON resistances of the MOSFETs Z1, Z2, Z3 and Z4 as the impedance elements need to be rendered small.

10 It has been found, however, that when the ON resistances (equivalent impedances) of the MOSFETs Z1 - Z4 within the common data line biasing circuit 60 are rendered small to the end of lowering the impedances of the common data lines L1 and L2, a through current I_x flowing through
15 the MOSFETs Z1 - Z4 in the non-selected mode (a current flowing in the direction of an arrow in the figure) increases this time, so a power consumption in this portion attributed to direct current augments.

That is, it has been revealed
20 that the contradictory problem occurs in which when the ON resistances of the MOSFETs within the common data line biasing circuit 60 are reduced for enhancing the operating speed, the power consumption in the non-selected mode increases this time.

A typical aspect of performance of the invention disclosed in the present application will be summarized below.

5 A voltage which is dropped by a fixed voltage from the highest operating potential in a memory device is divided by impedance elements, and common data lines are biased by the divided voltages.

10 By setting the resistances of the impedance elements at small values, time constants which are determined by the resistances and capacitances parasitic to the common data lines are reduced, whereby the potential changes of the common data lines arising in correspondence with the stored information of a memory cell are quickened to shorten a data sensing period of time and to enhance
15 an access time.

Since the voltage dropped by the fixed voltage from the highest operating voltage is applied, direct current to flow through the path of the impedance elements does not considerably increase in spite of the small
20 resistance values of these impedance elements, so that lowering in power consumption can be achieved.

According to a first aspect of the present invention there is provided a memory device including:

(a) a plurality of memory cells;

(b) a pair of common data lines coupled to said
5 plurality of memory cells for transmitting information stored in selected ones of said plurality of memory cells;

(c) a read-out circuit which is coupled to said pair of common data lines to receive said transmitted information and which generates output signals in response
10 to said transmitted information, wherein said read-out circuit includes a differential pair of bipolar transistors having their bases coupled to said pair of common data lines, respectively, and current source means coupled to said differential pair of bipolar transistors to provide operating
15 current to said differential pair of bipolar transistors;

(d) power supply means coupled to said plurality of memory cells, said power supply means having first and second potential levels, wherein said first potential level is different from said second potential level;

20 (e) a voltage generator circuit which is coupled to said power supply means and which generates an output voltage having a third potential level between said first and second potential levels; and

(f) a bias circuit connected to said pair of
25 common data lines, wherein the output voltage generated

by said voltage generator circuit is fed as a supply voltage to said bias circuit, and wherein said bias circuit includes means for biasing said pair of common data lines so that
5 said differential pair of bipolar transistors are operated in a non-saturation region when said memory device is selected for a read operation.

According to a second aspect of the present invention there is provided a memory device including:

10 (a) a plurality of memory cells;

(b) a read-out circuit including a pair of bipolar transistors for forming a sense circuit, said pair of bipolar transistors having bases;

(c) a pair of signal lines which are respectively
15 coupled to said bases of said pair of bipolar transistors of the read-out circuit and to said plurality of memory cells and which transmit complementary signals in accordance with data stored in selected ones of said memory cells to said bases of said pair of bipolar transistors of said read-out
20 circuit; and

(d) a biasing means comprising a voltage reducing circuit connected to a power source voltage for providing a predetermined voltage, the predetermined voltage having a value smaller than the value of said power source voltage,
25 and a bias circuit connected to said predetermined voltage for biasing said pair of signal lines at a predetermined bias voltage, the predetermined bias voltage having a value smaller than the value of said predetermined voltage so that

said pair of bipolar transistors are operated in a non-saturation region, wherein said voltage reducing circuit provides said predetermined voltage with a predetermined low
5 output impedance in response to a control signal.

According to a third aspect of the present invention there is provided a memory device including:

(a) a plurality of memory cells which store data therein;

10 (b) a plurality of word lines and a plurality of pairs of data lines coupled to said plurality of memory cells so that each memory cell is coupled to a word line and a pair of data lines;

(c) a pair of common data lines;

15 (d) switching means connected between said plurality of pairs of data lines and said pair of common data lines and for coupling a selected pair of one of said plurality of pair of data lines, to said pair of common data lines;

(e) an address circuit responsive to address signals
20 and coupled to said plurality of word lines and to said switching means and including means for selecting a predetermined memory cell in accordance with said address signals by selecting a predetermined word line and controlling said switching means to couple a predetermined
25 pair of data lines to said pair of common data lines;

(f) a sense circuit coupled to said pair of common data lines, said sense circuit coupled to said pair of common data lines, said sense circuit including a pair of

bipolar transistors that serve as a differential circuit having bases coupled to said pair of common data lines and current source means for providing operating current to said
5 differential circuit;

(h) a voltage generator having a bipolar transistor with a collector coupled to a first power terminal provided with a first power supply voltage of the memory device said voltage generator providing at an emitter of said bipolar
10 transistor a predetermined voltage smaller than said first power supply voltage;

(i) a pair of first MOSFETs which are respectively coupled between said emitter of said bipolar transistor and said pair of common data lines;

15 (j) a pair of second MOSFETs which are respectively coupled between said pair of common data lines and a second power terminal to which a second power supply voltage is supplied, said second power supply voltage being smaller than said first power supply voltage, wherein said pair of
20 common data lines are biased to a bias voltage between said predetermined voltage and said second power supply voltage so that said differential bipolar transistors are operated in non-saturation regions when said pair of first and second MOSFETs are turned on for a read operation.

25 The present invention will now be described in greater detail by way of examples with reference to the remaining figures of the accompanying drawings, wherein:

Fig. 3 is a diagram showing an example of the whole

arrangement of a memory device to which this invention is applied;

Fig. 4 is a diagram showing part of Fig. 3 and one 9d
5 embodiment in the essential portions of this invention;

Fig. 5 is a diagram showing an example of the characteristic of the memory device according to a first embodiment of this invention;

Fig. 6 is a circuit diagram of essential portions showing a second embodiment of this invention;

Fig. 7 is a circuit diagram of essential portions showing a third embodiment of this invention;

5 Fig. 8 is a circuit diagram of essential portions showing a fourth embodiment of this invention;

Fig. 9 is a diagram showing part of the circuit depicted in Fig. 8; and

10 Fig. 10 is a circuit diagram of essential portions showing another embodiment of this invention.

Referring to Fig. 3, the memory device 100 is constructed as the foregoing semiconductor integrated circuit of the so-called Bi/C-MOS type which has been developed by us and in which C-MOS elements and bipolar elements are formed coexistently, and it constructs
15 a static RAM in point of function. This semiconductor memory device 100 has a memory mat 10 in which a large number of memory cells M are arrayed in the shape of a matrix consisting of rows and columns, an X decoder/
20 driver 20 and a Y decoder 30 which serve to select the memory cell within the memory mat 10 on the basis of address data A_i , and so forth.

The X decoder/driver 20 decodes the lower (or upper) bit data of the address data A_i , to prepare alternative
25 select signals $X_0 - X_m$. The select signals $X_0 - X_m$

are applied to word lines W which are laid in the row direction of the memory mat 10.

The Y decoder 30 decodes the upper (or lower) bit data of the address data A_1 , to prepare alternative
5 select signals $Y_0 - Y_n$. The select signals $Y_0 - Y_n$ are applied to a Y select switch bank (column switch bank) 40. The Y select switch bank 40 operates to select any of complementary data line pairs D and $\bar{D}$, each pair
10 of complementary data lines being laid in the column direction of the memory mat 10. This selection is performed simultaneously with the selection of the word line W .

In the above way, the memory cells M within the memory mat 10 are respectively selected in the row direction and the column direction. The memory cell M , which
15 is connected in the place of intersection between the row and the column selected on the basis of the address data A_1 , is connected to common data lines $L1$ and $L2$ through the complementary data line pair D and $\bar{D}$ as well as the Y select switch bank 40. The change of
20 potentials appearing on the common data lines $L1$ and $L2$ is detected by a sense circuit 50, and the detected result becomes the read output D_{out} of stored data.

Fig. 4 shows part of the internal circuitry of the memory device illustrated in Fig. 3.

25 As shown in the figure, the memory cells M are

respectively connected to the pair of complementary data lines D and $\bar{D}$ of each column through MOS field effect transistors $m13$ and $m14$. The MOS field effect transistors $m13$, $m14$ interposed between the memory cell

5 M and the data lines D , $\bar{D}$ are turned ON (conductive) in the row direction by the selected word line W , while at the same time the data lines D , $\bar{D}$ of any column are selected, whereby the memory cell M located in the place of intersection between the selected word line W and

10 the selected data lines D , $\bar{D}$ is selected and is connected to the common data lines $L1$, $L2$. Each of the data lines D and $\bar{D}$ has one end thereof connected to a common power source V_{cc} through a MOS field effect transistor for pull-up $m11$ and has the other end thereof connected

15 to the common data line $L1$ or $L2$ through a Y select switch (column switch) $s1$ or $s2$ included in the Y switch bank 40. Accordingly, stored information written in the selected memory cell M can be read out in such a way that the change of the potentials complementarily

20 appearing on the common data lines $L1$ and $L2$ is detected by the sense circuit SA 50. The select switches $s1$ and $s2$ in the Y select switch bank are respectively constructed using MOS field effect transistors.

Meanwhile, in order to avoid the condition that

25 the common data lines $L1$ and $L2$ fall into floating states

and do not have their potentials fixed in a non-selected mode, a bias circuit 60 for applying fixed potentials to the common data lines L1 and L2 is disposed. The bias circuit 60 is so arranged that impedance elements
5 Z1, Z2, Z3 and Z4 formed of MOS field effect transistors are employed for assembling two sets of voltage divider circuits (Z1 and Z3, and Z2 and Z4), and that voltages at respective voltage division points are applied to the common data lines L1 and L2.

10 Here, the two sets of voltage divider circuits (bias circuit) (Z1 and Z3, and Z2 and Z4) are connected across the common power source V_{CC} and the ground potential with a voltage regulator circuit (also termed "constant voltage generator circuit" or "voltage drop generator circuit")
15 70 interposed in series therebetween. In this embodiment, the voltage regulator circuit 70 is constructed of a diode train D_n in which a plurality of diodes are connected in series in the forward direction. Thus, a power source V_d having a fixed voltage lower than that of the common
20 power source V_{CC} is provided. The lower source voltage V_d is applied to the respective voltage divider circuits (Z1 and Z3, and Z2 and Z4). Accordingly, the common data lines L1 and L2 are biased to fixed potentials by the voltages produced through the resistance division of
25 the lower source voltage V_d .

The MOS field effect transistors as the impedance elements Z1 - Z4 are respectively controlled to turn ON so as to have predetermined equivalent resistances (impedances) by fixed control voltages V_{s1} and V_{s2} .

5 The voltage divider circuits (Z1 and Z3, and Z2 and Z4) in the bias circuit 60 are fed with the voltage V_d which is dropped by a fixed voltage level from the supply voltage.

10 The potential V_{ref} of the common data lines L1 and L2 at the time at which the column switches s1 and s2 are not selected, becomes:

$$V_{ref} = (V_{cc} - n \cdot V_f) \cdot \frac{R3}{R1 + R3}$$

15 (or $V_{ref} = (V_{cc} - n \cdot V_f) \cdot \frac{R4}{R2 + R4}$)

where R1, R2, R3 and R4 denote the ON resistances of the MOS field effect transistors Z1, Z2, Z3 and Z4 as the impedance elements respectively.

20 On the other hand, the common data lines L1 and L2 are respectively connected to the bases of a differential pair of transistors Q1 and Q2 which constitute the sense amplifier SA 50. The minimum base potential V_b of the transistors Q1 and Q2 required for these transistors to stably turn ON is:

25 $V_b = V_{be} + V_{ds}$

where V_{ds} denotes the source-drain voltage of a MOS field effect transistor Q3 which operates as a constant current source for the differential transistors Q1 and Q2, and V_{be} the base-emitter voltage of the transistors Q1 and Q2.

Therefore, in order to bring the sense amplifier SA 50 into a stable operation state at high speed in the data reading mode, the common data line potential V_{ref} in the stand-by mode is set at a value which is lower than V_b by a certain voltage β .

That is, $V_{ref} = V_{be} + V_{ds} - \beta$ is set. The bias voltages which are applied to the bases of the transistors Q1 and Q2 are the minimum required potential, with which the transistor Q1 or Q2 is not saturated, and the output dynamic ranges of grounded-base transistors T27 and T28 which constitute the first amplifier stage of a data output intermediate amplifier DOIA do not narrow, either. The above explanation is illustrated in Fig. 5 as the potential switching characteristic of the common data lines L1 and L2.

Next, let's consider a case where the column switches s1 and s2 are turned ON by the Y select signal Y_0 so as to read out the data stored in the memory cell. In this case, the H (high) and L (low) information items of the data stored in the memory cell cause the potential

changes of the complementary data line pair D , $\bar{D}$ and the potential changes of the common data line pair $L1$, $L2$ and are then input to the sense amplifier SA 50. The situation of signal transfer on this occasion is depicted in the form of current changes in Fig. 4. While the actual signal transfer mechanism is affected by various factors and cannot be simply elucidated, Fig. 4 shall show the rough sketch thereof which will be briefly explained below.

10 Assuming now that an n-channel MOS field effect transistor m15 and MOS field effect transistor m16 which constitute the memory cell (flip-flop circuit) be in an OFF state and ON state respectively, the drain of the MOS field effect transistor m15 is at the "H" level, and that of the MOS field effect transistor m16 is at the "L" level. These potentials are respectively transmitted to the pair of complementary data lines D and $\bar{D}$ through the MOS field effect transistors m13 and m14, to render the data line D the "H" level and the data line $\bar{D}$ the "L" level.

Then, as regards the data line $\bar{D}$, charges stored through the precharging MOSFET m11 in a parasitic capacitance C_{s4} parasitic to this data line $\bar{D}$ are discharged to cause currents $I1$ and $I2$ to flow.

25 As regards the data line D , a current $I3$ flows

through the precharging MOSFET m11.

Next, the common data lines L1 and L2 will be considered. As regards the common data line L2, charges having been stored in a capacitance C_{s2} parasitic thereto are discharged principally through the MOSFET Z4 (current I6), so that the potential of the common data line L2 becomes the low level.

On the other hand, as regards the common data line L1, a capacitance C_{s1} parasitic thereto is charged with part of the current I3 and with a current I7 fed through the MOSFET Z1, so that the potential of the common data line L1 becomes the "H" level. The MOSFETs Z1, Z2, Z3 and Z4 participate in the charge and discharge of the parasitic capacitances C_{s1} and C_{s2} parasitic to the common data lines as briefly stated above, and the time constants which are determined by the equivalent resistances of the MOSFETs Z1 - Z4 and the parasitic capacitances C_{s1} , C_{s2} exert influences on the potential change speeds of the common data lines. As described before, therefore, the equivalent resistances of the MOSFETs Z1 - Z4 are set at the comparatively low values, owing to which the potential change speeds of the common data lines are raised. The inventors' study has revealed that the access time shortens when the equivalent resistances R1, R2, R3 and R4 of the respective MOSFETs Z1, Z2,

Z3 and Z4 are set to be $R1, R2 < R3, R4$.

Noteworthy here is that, even when the ON resistances of the MOSFETs Z1 - Z4 are lowered to some extent as described above, the voltage V_d lowered by the certain
5 voltage from the supply voltage V_{cc} is provided from the voltage regulator circuit 70 and is applied to the drains of the MOSFETs Z1 and Z2, whereby the magnitudes of through currents (direct currents) which flow through the MOSFETs Z1, Z3 and those Z2, Z4 in the non-selected
10 mode can be made small.

As thus far stated, the common data line potential is lowered and the equivalent impedances of the common data lines L1, L2 are reduced without causing any great through current or steady current to flow, so that the
15 operating speed can be enhanced whilst suppressing the power consumption. That is, the time constants dependent upon the parasitic capacitances near the common data lines L1, L2 decrease owing to the lowered impedances of these common data lines L1, L2, whereby the enhancement
20 of the operating speed can be achieved.

Fig. 5 shows the situation of potential change-over in the common data lines L1 and L2.

Fig. 6 shows a second embodiment in the essential portions of the memory device according to this invention.

25 The embodiment shown in the figure is basically

the same as the foregoing embodiment. Herein, however, the output stage of a constant voltage generator circuit which serves to produce the lower source voltage V_d for operating the bias circuit 60 is provided with an
5 emitter follower so as to realize a low output impedance.

When the output impedance of the constant voltage generator circuit 72 is lowered in this manner, an output voltage signal can be reliably fed to the bias circuit 60 even if a signal transmission line L3 coupling the
10 constant voltage generator circuit and the bias circuit becomes long. As a result, in designing the layout of an IC, it is also possible to arrange only the constant voltage generator circuit 72 in a convenient place independently and to transmit the output voltage thereof to the common
15 data line biasing circuit 60 by means of A1 wiring or the like. This enhances versatility in the layout design.

Moreover, in an arrangement in which the memory cells and the common data lines are divided into several groups, the divided groups of common data lines can share the
20 single constant voltage generator circuit 72. This is useful for reducing a chip area.

The constant voltage generator circuit 72 is constructed using the emitter follower stage which is composed of a bipolar transistor Q71 and a MOS field effect transistor
25 m74. The MOS field effect transistor m74 in this case

functions as a load impedance. This load impedance is set sufficiently higher than that of the impedance elements Z1 - Z4 in order to prevent a consumption current in the emitter follower stage from increasing. Besides,
5 MOS field effect transistors m71, m72 and m73 and a diode train D_n are used for applying a reference voltage to the emitter follower stage.

Here, when a fixed current is fed to the diode train D_n by the conduction of the MOS field effect transistors
10 m71, m72 and m73, a fixed voltage develops across both the ends of the diode train D_n . This fixed voltage is input to the base of the bipolar transistor Q71, the emitter of which responsively provides the power source V_d of low impedance output. The voltage of the output
15 power source V_d is set sufficiently lower than that of the common power source V_{cc} by adjusting the number of the diodes of the diode train D_n , etc., whereby the bias circuit 60 composed of the impedance elements Z1 - Z4 can be furnished with the power source V_d of low voltage
20 and low impedance. Thus, the same effect as in the foregoing embodiment can be attained.

Further, in the embodiment shown in Fig. 6, the MOS field effect transistors m71, m72 for causing the fixed current to flow through the diode train D_n and
25 the MOS field effect transistor m74 as the load resistance

of the bipolar transistor Q71 are respectively controlled by external signals including, for example, a chip select signal $\overline{CS}$. This can realize an arrangement wherein, in the stand-by mode (with $\overline{CS}$ being "H") by way of example, the MOS field effect transistors m71, m72 and m74 are brought into OFF states so as to automatically turn OFF the operating power source V_d of the bias circuit 60. Thus, it is permitted to automatically save power consumption during, for example, any mode other than the reading operation or the non-selected mode.

Fig. 7 shows a third embodiment in the essential portions of the memory device according to this invention.

Likewise to the embodiment shown in Fig. 6, the embodiment shown in Fig. 7 is also provided with a constant voltage generator circuit 72 based on an emitter follower in order to afford the power source V_d of low voltage and low output impedance for operating the bias circuit 60.

This constant voltage generator circuit 72 is constructed using the emitter follower stage which is composed of a bipolar transistor Q71 and a MOS field effect transistor m74. The MOS field effect transistor m74 in this case functions as a load impedance, and acts to stabilize the potential. In addition, p-channel depletion-mode MOS field effect transistors m71 and m72 and fixed voltage generating diodes D_{d1} and D_{d2} are used for applying

a reference voltage to the emitter follower stage.

Here, when a fixed current I flows through the diodes D_{d1} and D_{d2} via the depletion-mode MOS field effect transistors $m71$ and $m72$, the emitter of the bipolar transistor $Q71$ produces the voltage V_d which is determined by $V_{cc} - I \cdot R71 - V_{BEQ71}$ (where $R71$ denotes the ON resistance of the MOSFET $m71$, and V_{BEQ71} the base-emitter voltage of the transistor $Q71$) and which is of low impedance output. By setting the output voltage V_d to be lower than the voltage of the common power source V_{cc} , the bias circuit 60 composed of the impedance elements $Z1 - Z4$ can be furnished with the power source V_d of low voltage and low impedance. Thus, the same effect as in the foregoing embodiments can be attained.

Further, in the embodiment shown in Fig. 7, the diodes D_{d1} and D_{d2} function to compensate the temperature dependence of the base-emitter voltage of the transistor $Q71$ and prevent the output voltage V_d from fluctuating in correspondence with a temperature change. In consequence, the output voltage (V_d) is stabilized against temperatures. Thus, the bias potentials of the common data lines $L1$ and $L2$ can be more stabilized. This makes it possible to perform stable and reliable read-out sensing even when, by way of example, the amplitudes of signal voltages on the common data lines $L1$ and $L2$ are sharply reduced.

Fig. 8 shows a fourth embodiment in the essential portions of the memory device according to this invention.

Unlike the preceding embodiments, the embodiment shown in the figure has a bias circuit 60 constructed without employing a resistance voltage divider circuit. Here, the output of a constant voltage generator circuit 72 of low voltage and low impedance output as left intact is applied to the common data lines L1 and L2 through impedance elements Z1 and Z2 respectively. In this case, the constant voltage generator circuit 72 is constructed of an active circuit which simulates an ideal battery. That is, the constant voltage generator circuit 72 is used which has no directivity in impedance, namely, which has a bidirectional output characteristic wherein a fixed low impedance is exhibited in both a case where an outflow current (discharge current) I_{x0} flows and a case where an inflow current (absorption current) I_{xi} flows.

Fig. 9 shows an example of the constant voltage generator circuit 72 which has the bidirectional output characteristic. The constant voltage generator circuit 72 shown in the figure constructs an active circuit of the so-called voltage follower by the use of a differential type high gain D. C. amplifier circuit 74. A very high equivalent impedance is attained on the input side of this active circuit, and a very low equivalent impedance

on the output side thereof. Accordingly, when a voltage obtained by dividing the voltage of the common power source V_{cc} by means of high resistances $R1$ and $R2$ is input, a D. C. output which is substantially the same
5 voltage as this input voltage is produced with a low output impedance. Thus, the common data lines $L1$ and $L2$ can be biased into low impedance states without causing a great steady current or through current to flow. Moreover, the bias potential can be set as desired in accordance
10 with the ratio between the high resistances $R1$ and $R2$. This makes it possible to bias the common data lines $L1$ and $L2$ into states which are the most suitable for high speed reading and stable operations.

In this embodiment, the output voltage (V_d) of
15 the constant voltage generator circuit 72 is set sufficiently lower than the voltage of the common power source V_{cc} . Concretely, it is set at a voltage which can ensure a potential difference capable of rendering sufficiently
low the ON (conduction) resistances of the MOS field
20 effect transistors that are used as the Y select switches $s1$, $s2$ between the data lines D , $\bar{D}$ and the common data lines $L1$, $L2$.

Fig. 10 shows a static memory device of 64 kilobits according to this invention.

25 The embodiment shown in the figure is so constructed

that stored information written a selected memory cell M-CEL is read out through common data lines L1, L2 and a read-out sensing circuit SA 50, and that the common data lines L1, L2 and the read-out sensing circuits

5 SA 50 are dividedly disposed in a plurality of groups. In this 64 k-bit RAM, the common data lines L1, L2 and the read-out sensing circuits 50 are provided in a manner to be divided into 16 groups, any of which is selected and activated. A circuit of logic symbol in Fig. 10,

10 the output side of which is marked in black, is a quasi-CMOS circuit in which an output transistor for charging and discharging the stray capacitance of an output signal line is formed of a bipolar transistor and in which logic processing such as inversion, non-inversion, NAND

15 or NOR is executed by a CMOS circuit, whereas a circuit of ordinary logic symbol is a pure CMOS circuit. As illustrated in Fig. 10, in an address buffer ADB, there are arranged non-inverting and inverting circuits G7 - G15 whose inputs receive address signals A7 - A15

20 of TTL levels from outside by way of example and which serve to deliver non-inverted outputs a7 - a15 and inverted outputs $\bar{a}7 - \bar{a}15$ to complementary output signal lines. The output transistors of the non-inverting and inverting circuits G7 - G15 are formed of the bipolar transistors

25 as stated above, so that even when the output signal

lines of the non-inverting and inverting circuits G7 - G15 are arranged over a long distance on the surface of a semiconductor chip, these non-inverting and inverting circuits G7 - G15 can be operated at high speed.

5 Next, a Y decoder Y-DCR1 will be briefly explained.

It includes 2-input NAND circuits G74 - G77, G78 - G81 and G82 - G85 and 3-input NAND circuits G86 - G93 to which the internal address signals $a_7 - a_{15}$ and $\bar{a}_7 - \bar{a}_{15}$ provided from the address buffer ADB are applied.

10 Further, in the Y decoder Y-DCR1, the output signal lines of the NAND circuits G74 - G93 are arranged at long distances and are connected to the input terminals of a large number of NOR circuits G94 - G95, so that the stray capacitances of the output signal lines of
15 these NAND circuits G74 - G93 become large capacitance values.

Accordingly, the 3-input NAND circuits G86 - G93 are constructed of quasi-CMOS 3-input NAND circuits whose output transistors are bipolar, while the 2-input
20 NAND circuits G74 - G85 are constructed of quasi-CMOS 2-input NAND circuits whose output transistors are bipolar.

On the other hand, in Fig. 10, the output signal lines of the 3-input NOR circuits G94 - G95 are connected to the inputs of inverters G100 - G101 at a short distance,
25 so that the stray capacitances of the output signal lines

of these 3-input NOR circuits G94 - G95 have small capacitance values. Accordingly, these 3-input NOR circuits G94 - G95 are constructed of pure CMOS 3-input NOR circuits.

Further, since the output signal lines of the inverters
5 G100 - G101 are connected to the input terminals of
2-input NOR circuits G98 - G99 at a short distance, the
capacitance values of the stray capacitances of the output
signal lines of these inverters G100 - G101 are small.
Accordingly, these inverters G100 - G101 are constructed
10 of well-known pure CMOS inverters.

There will now be explained the memory cell M-CEL
of 1 bit which constitutes a memory array M-ARY.

This memory cell M-CEL is constructed of a flip-
flop in which the inputs and outputs of a pair of inverters
15 composed of load resistances R1, R2 and n-channel MISFETs
Q101, Q102 are cross-connected, and n-channel MISFETs
Q103, Q104 for transfer gates.

The flip-flop is used as means for storing information.
The transfer gates are controlled by an address signal
20 which is applied to a word line X_1 connected to an X
decoder (row decoder), and the information transfer
between a complementary data line pair D1001, $\bar{D}1001$
and the flip-flop is controlled by these transfer gates.

In the reading operation, MOS field effect transistors
25 m1 and m2 are brought into OFF states by a write enable

control signal WECS, and the information stored in the memory cell is read out through a data output buffer DOB as well as the read-out sense circuit SA 50 which is activated by a read-out sense circuit select signal Y_s generated from a read-out sense circuit selecting circuit SASC (and a chip select signal $\overline{CS}$).

In the writing operation, the MOS field effect transistors m1 and m2 are brought into ON states, whereas the read-out sense circuit SA 50 is brought into an OFF state by a read-out sense circuit select signal Y_s' . Thus, input data is written into a predetermined memory cell through a data input buffer DIB and a data input intermediate amplifier circuit DIIA.

According to the embodiment shown in Fig. 10, the memory device 100 of the above arrangement is characterized in that only the common data lines L1, L2 connected to the read-out sense circuit 50 of the selected group are selectively fed with voltages for biasing these data lines to a fixed potential. Concretely, the bias circuit 60 is provided for the common data lines L1, L2 and read-out sense circuit 50 of each group. Simultaneously therewith, the select signal Y_s of the read-out sense circuit 50 is branched, and the branched signal is used as the control signal of the bias circuit 60. Only ground side impedance elements Z3, Z4 within the bias

circuit 60 corresponding to the selected read-out sense circuit 50 are brought into ON states, and all the other ground side impedance elements within the bias circuits 60 corresponding to the non-selected read-out sense circuits 5 (not shown) are brought into OFF states. In this way, a current for biasing the common data lines L1, L2 can be reduced down to about 1/16 in the case of the aforementioned 64 k-bit RAM by way of example. Further, the select signal Y_s of the read-out sense circuit has its logical product taken with the chip select signal CS. On this 10 occasion, the current for biasing the common data lines L1, L2 is permitted to scarcely flow in the stand-by mode during which the chip select signal CS is inactive. Thus, according to this embodiment, the average power 15 consumption of the memory device 100 can be saved more.

A constant voltage generator circuit 72 for applying a low voltage V_d to the bias circuit 60 has its output rendered a low impedance output utilizing a voltage follower, whereby the stray capacitances and other parasitic 20 impedances of signal transfer lines can be neglected, and only one constant voltage generator circuit 72 disposed in the IC can be exploited in common.

The effects of the present invention thus far described will be summed up below.

25 (1) In a memory device which is so constructed that

stored information written in a selected memory cell is read out through common data lines, the equivalent impedances of the common data lines can be sharply reduced without causing a great through current or steady current to flow. This achieves the effect that an operating speed can be enhanced without considerably increasing a power consumption.

(2) In a memory device which is so constructed that stored information written in a selected memory cell is read out through common data lines and a read-out sense circuit and that the common data lines and the read-out sense circuits are dividedly disposed in a plurality of groups, only the read-out sense circuit of one of the plurality of groups being selected and activated; only the common data lines connected to the read-out sense circuit of the selected group are selectively fed with voltages for biasing these data lines to a fixed potential, whereby a current for biasing the common data lines can be lessened still sharply. This achieves the effect that the average power consumption of the entire memory device can be saved more.

While, in the above, the invention made by the inventors has been concretely described in conjunction with embodiments, it is needless to say that this invention is not restricted to the foregoing embodiments but that

it can be variously modified within a scope not departing from the subject matter thereof. For example, bipolar transistors may well be employed for the impedance elements Z1 - Z4 within the bias circuit 60.

5 While, in the above, the invention made by the inventors has been chiefly explained as to the case of application to a static RAM which forms the background field of utilization thereof, it is not restricted thereto but is also applicable to a ROM or a dynamic RAM by way
10 of example. The invention is applicable to any device including at least the condition that stored information is read out through common data lines.



CLAIMS:-

1. A memory device including:
 - (a) a plurality of memory cells;
 - (b) a pair of common data lines coupled to said plurality of memory cells for transmitting information stored in selected ones of said plurality of memory cells;
 - (c) a read-out circuit which is coupled to said pair of common data lines to receive said transmitted information and which generates output signals in response to said transmitted information, wherein said read-out circuit includes a differential pair of bipolar transistors having their bases coupled to said pair of common data lines, respectively, and current source means coupled to said differential pair of bipolar transistors to provide operating current to said differential pair of bipolar transistors;
 - (d) power supply means coupled to said plurality of memory cells, said power supply means having first and second potential levels, wherein said first potential level is different from said second potential level;
 - (e) a voltage generator circuit which is coupled to said power supply means and which generates an output voltage having a third potential level between said first and second potential levels; and
 - (f) a bias circuit connected to said pair of common data lines, wherein the output voltage generated by said voltage generator circuit is fed as a supply



voltage to said bias circuit, and wherein said bias circuit includes means for biasing said pair of common data lines so that said differential pair of bipolar transistors are operated in a non-saturation region when said memory device is selected for a read operation.

2. A memory device according to claim 1, wherein said bias circuit is a voltage divider circuit which is composed of a plurality of impedance elements, the output voltage generated by said voltage generator circuit is divided by said impedance elements, and said pair of common data lines are biased to a predetermined potential by the divided voltages.

3. A memory device according to claim 2, wherein said impedance elements are MIS field effect transistors.

4. A memory device according to claim 1, wherein said voltage generator circuit has an arrangement in which diodes are connected in series.

5. A memory device according to claim 1, wherein said voltage generator circuit generates the output of low impedance.

6. A memory device according to claim 5, wherein said voltage generator circuit is a voltage follower.

7. A memory device according to claim 5, wherein said voltage generator circuit is constructed of bipolar and MIS field effect transistors in combination.



8. A memory device according to claim 1, wherein each memory cell is a flip-flop which is composed of MISFETs.

9. A memory device according to claim 1, wherein the memory cells, the common data lines and the bias circuits are disposed in a manner to be divided in a plurality of groups, and wherein the output of said voltage generator circuit is shared and utilized by said bias circuits which are provided for the respective common data lines of the corresponding groups.

10. A memory device according to claim 9, wherein said output of said voltage generator circuit is of low output impedance.

11. A memory device including:

(a) a plurality of memory cells;

(b) a read-out circuit including a pair of bipolar transistors for forming a sense circuit, said pair of bipolar transistors having bases;

(c) a pair of signal lines which are respectively coupled to said bases of said pair of bipolar transistors of the read-out circuit and to said plurality of memory cells and which transmit complementary signals in accordance with data stored in selected ones of said memory cells to said bases of said pair of bipolar transistors of said read-out circuit; and



(d) a biasing means comprising a voltage reducing circuit connected to a power source voltage for providing a predetermined voltage, the predetermined voltage having a value smaller than the value of said power source voltage, and a bias circuit connected to said predetermined voltage for biasing said pair of signal lines at a predetermined bias voltage, the predetermined bias voltage having a value smaller than the value of said predetermined voltage so that said pair of bipolar transistors are operated in a non-saturation region, wherein said voltage reducing circuit provides said predetermined voltage with a predetermined low output impedance in response to a control signal.

12. A memory device according to claim 11, wherein said bias circuit comprises a voltage divider to which said predetermined voltage is fed.

13. A memory device according to claim 11, wherein said voltage reducing circuit comprises an emitter follower transistor.

14. A memory device according to claim 11, wherein each memory cell includes a pair of N-channel MOSFETs having their gates and drains cross-coupled.

15. A memory device according to claim 11, wherein said control signal is based on a signal for indicating a chip selected mode.



16. A memory device including:

(a) a plurality of memory cells which store data therein;

5 (b) a plurality of word lines and a plurality of pairs of data lines coupled to said plurality of memory cells so that each memory cell is coupled to a word line and a pair of data lines;

(c) a pair of common data lines;

10 (d) switching means connected between said plurality of pairs of data lines and said pair of common data lines and for coupling a selected pair of one of said plurality of pair of data lines, to said pair of common data lines;

(e) an address circuit responsive to address signals
15 and coupled to said plurality of word lines and to said switching means and including means for selecting a predetermined memory cell in accordance with said address signals by selecting a predetermined word line and controlling said switching means to couple a predetermined
20 pair of data lines to said pair of common data lines;

(f) a sense circuit coupled to said pair of common data lines, said sense circuit coupled to said pair of common data lines, said sense circuit including a pair of bipolar transistors that serve as a differential circuit
25 having bases coupled to said pair of common data lines and current source means for providing operating current to said differential circuit;

(h) a voltage generator having a bipolar transistor



with a collector coupled to a first power terminal provided with a first power supply voltage of the memory device said voltage generator providing at an emitter of said bipolar transistor a predetermined voltage smaller than said first power supply voltage;

(i) a pair of first MOSFETs which are respectively coupled between said emitter of said bipolar transistor and said pair of common data lines;

(j) a pair of second MOSFETs which are respectively coupled between said pair of common data lines and a second power terminal to which a second power supply voltage is supplied, said second power supply voltage being smaller than said first power supply voltage, wherein said pair of common data lines are biased to a bias voltage between said predetermined voltage and said second power supply voltage so that said differential bipolar transistors are operated in non-saturation regions when said pair of first and second MOSFETs are turned on for a read operation.

17. A memory device according to claim 16, wherein said plurality of memory cells have static type memory cells each of which has a flip-flop circuit composed of a pair of N-channel MOSFETs and load elements.

18. A memory device according to claim 16, wherein said voltage generator has a control terminal for receiving a control signal indicating a chip selection mode so that



said voltage generator generates said predetermined voltage when a chip is selected.

19. A memory device according to claim 16, wherein gate
5 electrodes of said pair of first MOSFETs are coupled to receive a timing signal and wherein gate electrodes of said pair of second MOSFETs are coupled to receive a sense circuit activation signal.
20. A memory device according to claim 16, wherein said
10 current source means includes a third MOSFET with a source-drain path coupled between said emitters of said differential bipolar transistors and said second power terminal.
21. A memory device according to claim 16, wherein said
15 differential bipolar transistors are NPN transistors.
22. A memory device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Fig. 4 to Fig. 10 of the accompanying drawings.
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