CLAIMS:

1. An integrated circuit structure, comprising:

an NMOS transistor comprising:

a first dielectric spacer and a second dielectric spacer over a first fin, wherein the first dielectric spacer has an upper surface, and the second dielectric spacer has an upper surface;

a first gate dielectric layer over the first fin between the first dielectric spacer and the second dielectric spacer, wherein the first gate dielectric layer extends along a portion of the first dielectric spacer and extends along a portion of the second dielectric spacer, wherein the first gate dielectric layer has an upper surface below the upper surface of the first dielectric spacer and below the upper surface of the second dielectric spacer, and wherein the first gate dielectric layer comprises hafnium and oxygen;

a first gate electrode over the first gate dielectric layer between the first dielectric spacer and the second dielectric spacer, wherein the first gate electrode extends along a portion of the first dielectric spacer and extends along a portion of the second dielectric spacer, wherein the first gate electrode includes a layer comprising titanium, aluminum and carbon, and wherein the layer of first gate electrode has an upper surface below the upper surface of the first dielectric spacer and below the upper surface of the second dielectric spacer; and

a gate capping dielectric structure between and in contact with the first dielectric spacer and the second dielectric spacer, wherein the gate capping dielectric structure is directly on the upper surface of the first gate dielectric layer and directly on the upper surface of the first gate electrode, and wherein the gate capping layer comprises silicon and nitrogen; and

a PMOS transistor comprising:

a second gate dielectric layer over a second fin, wherein the second gate dielectric layer comprises hafnium and oxygen; and

a second gate electrode over the second gate dielectric layer, wherein the second gate electrode does not include a layer comprising titanium, aluminum and carbon, and wherein the second gate electrode includes a layer comprising titanium and nitrogen.

2. The integrated circuit structure of claim 1, wherein the first gate electrode further comprises a gate fill barrier layer on the layer comprising titanium, aluminum and carbon, wherein the gate fill barrier layer comprises titanium and nitrogen, and wherein the gate capping dielectric structure is on an upper surface of the gate fill barrier layer.

3. The integrated circuit structure of claim 2, wherein the first gate electrode further comprises a gate fill material on the gate fill barrier layer, wherein the gate fill material comprises tungsten, and wherein the gate capping dielectric structure is on an upper surface of the gate fill material.

4. The integrated circuit structure of claim 1, wherein the first fin and the second fin comprise silicon.

5. The integrated circuit structure of claim 1, wherein the layer comprising titanium, aluminum and carbon comprises between 20% and 40% by weight aluminum.

6. The integrated circuit structure of claim 1, wherein the layer comprising titanium, aluminum and carbon comprises between 30% and 50% by weight titanium.

7. The integrated circuit structure of claim 1, wherein the layer comprising titanium, aluminum and carbon comprises between 10% and 30% by weight carbon.

8. The integrated circuit structure of claim 1, wherein the layer comprising titanium, aluminum and carbon comprises between 20% and 40% by weight aluminum, comprises between 30% and 50% by weight titanium, and comprises between 10% and 30% by weight carbon.

9. The integrated circuit structure of claim 1, wherein the layer comprising titanium, aluminum and carbon comprises about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon.

10. The integrated circuit structure of claim 1, wherein the gate capping dielectric structure comprises silicon nitride.

11. A method of fabricating an integrated circuit structure, the method comprising:

forming an NMOS transistor, the forming comprising:

forming a first dielectric spacer and a second dielectric spacer over a first fin, wherein the first dielectric spacer has an upper surface, and the second dielectric spacer has an upper surface;

forming a first gate dielectric layer over the first fin between the first dielectric spacer and the second dielectric spacer, wherein the first gate dielectric layer extends along a portion of the first dielectric spacer and extends along a portion of the second

dielectric spacer, wherein the first gate dielectric layer has an upper surface below the upper surface of the first dielectric spacer and below the upper surface of the second dielectric spacer, and wherein the first gate dielectric layer comprises hafnium and oxygen;

forming a first gate electrode over the first gate dielectric layer between the first dielectric spacer and the second dielectric spacer, wherein the first gate electrode extends along a portion of the first dielectric spacer and extends along a portion of the second dielectric spacer, wherein the first gate electrode includes a layer comprising titanium, aluminum and carbon, and wherein the layer of first gate electrode has an upper surface below the upper surface of the first dielectric spacer and below the upper surface of the second dielectric spacer; and

forming a gate capping dielectric structure between and in contact with the first dielectric spacer and the second dielectric spacer, wherein the gate capping dielectric structure is directly on the upper surface of the first gate dielectric layer and directly on the upper surface of the first gate electrode, and wherein the gate capping layer comprises silicon and nitrogen; and

forming a PMOS transistor comprising:

forming a second gate dielectric layer over a second fin, wherein the second gate dielectric layer comprises hafnium and oxygen; and

forming a second gate electrode over the second gate dielectric layer, wherein the second gate electrode does not include a layer comprising titanium, aluminum and carbon, and wherein the second gate electrode includes a layer comprising titanium and nitrogen.

12. The method of claim 11, wherein the first gate electrode further comprises a gate fill barrier layer on the layer comprising titanium, aluminum and carbon, wherein the gate fill barrier layer comprises titanium and nitrogen, and wherein the gate capping dielectric structure is on an upper surface of the gate fill barrier layer.

13. The method of claim 12, wherein the first gate electrode further comprises a gate fill material on the gate fill barrier layer, wherein the gate fill material comprises tungsten, and wherein the gate capping dielectric structure is on an upper surface of the gate fill material.

14. The method of claim 11, wherein the first fin and the second fin comprise silicon.

15. The method of claim 11, wherein the layer comprising titanium, aluminum and carbon comprises between 20% and 40% by weight aluminum.

16. The method of claim 11, wherein the layer comprising titanium, aluminum and carbon comprises between 30% and 50% by weight titanium.

17. The method of claim 11, wherein the layer comprising titanium, aluminum and carbon comprises between 10% and 30% by weight carbon.

18. The method of claim 11, wherein the layer comprising titanium, aluminum and carbon comprises between 20% and 40% by weight aluminum, comprises between 30% and 50% by weight titanium, and comprises between 10% and 30% by weight carbon.

19. The method of claim 11, wherein the layer comprising titanium, aluminum and carbon comprises about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon.

20. The method of claim 11, wherein the gate capping dielectric structure comprises silicon nitride.