portion 35A located above the bottom end of the semiconductor film 31, and a portion 35B located below the bottom end of the semiconductor film 31. As compared to the n^+-type impurity diffusion region 33, the portion 35A of the n^+-type impurity diffusion region 35 is provided in a position farther from the center of the memory pillar MP.

The n^+-type impurity diffusion region 33 is located above the bottom end of the semiconductor film 31, and at an approximately central portion of the memory pillar MP. The n^+-type impurity diffusion region 33 is in contact with a portion 35B of the n^+-type impurity diffusion region 35, and is separated from the portion 35A.

The semiconductor portion 36 covers the upper surface of the core member 30, and is in contact with an inner wall portion of the semiconductor film 31 above the core member 30. The semiconductor portion 36 has, for example, a columnar shape, and reaches the top end of the upper pillar UMP.

On the upper surface of the semiconductor film 31 and the semiconductor portion 36 in the memory pillar MP, a conductive layer 24 that functions as a columnar contact CP is provided. The conductive layer 24 includes, for example, tungsten (W). The cross-sectional view of FIG. 4 illustrates a contact CP corresponding to one memory pillar MP of the two memory pillars MP. In the other memory pillar MP on which no contact CP is shown, the contact CP is provided in a cross section in back or in front in the depth direction of the plane of paper of FIG. 4. An upper

surface of each contact CP is in contact with and electrically coupled to the corresponding one conductive layer 25 (bit line BL).

The insulating layer 37 is formed in, for example, a plate shape extending along the XZ plane and functions as a slit SLT that divides the conductive layers 21 to 23 along the Y axis. The insulating layer 37 divides the conductive layers 21 to 23 into blocks BLK for example. A top end of the insulating layer 37 is located between the conductive layer 23 and the conductive layer 25, and a bottom end of the insulating layer 37 is located below the lowermost conductive layer 21. The insulating layer 37 includes an insulator such as silicon oxide (SiO_2).

The insulating layer 38 is formed in, for example, a plate shape extending along the XZ plane and functions as a slit SHE that divides the conductive layer 23 along the Y direction. The insulating layer 38 divides the conductive layer 23 into string units SU for example. A top end of the insulating layer 38 is located between the conductive layer 23 and the conductive layer 25, and a bottom end of the insulating layer 38 is located, for example, between the conductive layer 23 and the uppermost conductive layer 22. The insulating layer 38 includes an insulator such as silicon oxide (SiO_2).

Next, a cross-sectional structure of the lower pillar LMP and the upper pillar UMP along the XY plane will be

the capacitor CAP. On the other hand, when the selected memory cell transistor MT is in the OFF state, the voltage at the node N2 of the bit line BL that is in conduction with the NAND string NS does not substantially change. The sense amplifier module 16 senses a difference in voltage change at the node N2, thereby reading the data stored in the selected memory cell transistor MTo.

To sense a difference in voltage change of the bit line BLo with high accuracy in the read operation described above, it is preferable that the capacitance of the capacitor CAP be about 10% or more of the capacitance of the bit line BL. In other words, it is preferable that the capacitance of the capacitor CAP be as large as possible, while the capacitance of the bit line BL be as small as possible.

According to the embodiment, the n^+-type impurity diffusion region 35 includes the portion 35A located above the bottom end of the semiconductor film 31, and the portion 35B located below the bottom end of the semiconductor film 31. Furthermore, the n^+-type impurity diffusion region 33 is located above the bottom end of the semiconductor film 31, in contact with the portion 35B, and separated from the portion 35A. Accordingly, the semiconductor film 31 in the bottom portion BTM has a cylindrical shape, and the inner surface, the bottom surface, and the outer surface of the cylindrical shape can function as an electrode of the capacitor CAP. Therefore,