~~What is claimed is:~~

1. A method of preventing crack propagation in the fabrication of an integrated circuit device comprising:

providing a plurality of integrated circuits on a wafer;

fabricating dummy metal lines in corner regions of each of said plurality of integrated circuits; and

separating said plurality of integrated circuits from one another wherein said separating produces cracks in said corner regions of said plurality of integrated circuits and wherein said dummy metal lines prevent propagation of said cracks in said corner regions .

2. The method according to Claim 1 wherein said dummy metal lines comprise copper.

3. The method according to Claim 1 further comprising fabricating dummy semiconductor devices wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy semiconductor devices and an active area of a substrate of one of said plurality of integrated circuits.

4. The method according to Claim 3 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

5. The method according to Claim 1 wherein said separating step comprises wafer sawing or wafer dicing.

6. The method according to Claim 1 wherein low dielectric constant dielectric material separates conducting layers from one another.

7. The method according to Claim 1 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

8. A method of preventing crack propagation in the fabrication of an integrated circuit device comprising:

providing a plurality of integrated circuits on a wafer;

fabricating dummy semiconductor devices and dummy metal lines in corner regions of each of said plurality of integrated circuits wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy semiconductor devices and an active area of a semiconductor substrate of one of said plurality of integrated circuits; and

separating said plurality of integrated circuits from one another wherein said separating produces cracks in said corner regions of said plurality of integrated circuits and wherein said dummy metal lines prevent propagation of said cracks in said corner regions .

9. The method according to Claim 8 wherein said dummy metal lines comprise copper.

10. The method according to Claim 8 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

~~11. The method according to Claim 8 wherein low dielectric constant dielectric material~~ separates conducting layers from one another.

12. The method according to Claim 8 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

13. The method according to Claim 8 wherein said separating step comprises wafer sawing or wafer dicing.

14. A semiconductor wafer comprising:

a plurality of integrated circuits on said semiconductor wafer wherein each of said integrated circuits contains semiconductor devices; and

dummy metal lines in corner regions of each of said plurality of integrated circuits wherein said dummy metal lines prevent propagation of cracks in said corner regions of each of said plurality of integrated circuits.

15. The wafer according to Claim 14 wherein said dummy metal lines comprise copper.

16. The wafer according to Claim 14 further comprising dummy semiconductor devices wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said

dummy semiconductor device and an active area of a semiconductor substrate of one of said plurality of integrated circuits.

17. The wafer according to Claim 16 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

18. The wafer according to Claim 14 wherein low dielectric constant dielectric material separates conducting layers from one another.

19. The wafer according to Claim 14 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

20. A method for forming dummy features in corner regions of a plurality of integrated circuits on a wafer, said method comprising:

generating a layout of said dummy features comprising:

for each of said plurality of integrated circuits on said wafer:

locating four corners of said integrated circuit;

creating a square of a first size in each of said four corners within which said dummy features will be created; and

within each square:

finding semiconductor features within said square;

marking areas of said square not containing said semiconductor features wherein said marked areas are located away from said found semiconductor features by a buffer area;

generating alternating grid squares of a second size smaller than said first size;

expanding said alternating grid squares to form rectangles;

generating a dummy active area within said marked areas by merging said rectangles to form a grid; and

generating anchored contacts and vias within said dummy active area;

mapping each level of generated said dummy active area from each of said squares to a mask; and

forming said dummy features in conjunction with formation of real circuit features to complete fabrication of said integrated circuits..

21. The method according to Claim 20 wherein said dummy features comprise copper.

22. The method according to Claim 20 further comprising separating said plurality of integrated circuits from one another wherein said separating produces cracks in said corner regions of said plurality of integrated circuits and wherein said dummy features prevent propagation of cracks in corner regions of each of said plurality of integrated circuits.

~~23. The method according to Claim 22 wherein said separating comprises wafer sawing or~~ wafer dicing.

24. The method according to Claim 20 wherein low dielectric constant dielectric material separates conducting layers from one another.

25. The method according to Claim 20 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy features.

26. A method in a data processing system for generating a layout of dummy features in corner regions of a plurality of integrated circuits on a wafer, said method comprising:

for each of said plurality of integrated circuits on said wafer:

locating four corners of said integrated circuit;

creating a square of a first size in each of said four corners within which said dummy features will be created; and

within each square:

finding semiconductor features within said square;

marking areas of said square not containing said semiconductor features wherein said marked areas are located away from said found semiconductor features by a buffer area;

generating alternating grid squares of a second size smaller than said first size;

expanding said alternating grid squares to form rectangles;

generating a dummy active area within said marked areas by merging said rectangles to form a grid; and

generating anchored contacts and vias within said dummy active area; and

mapping generated said dummy active area from each of said squares to a mask to complete generation of said dummy layout.

What is claimed is:

1. A method of fabricating an integrated circuit device comprising:

providing a plurality of integrated circuits on a wafer;

fabricating a dummy structure in a corner region of each of said plurality of integrated circuits comprising:

fabricating dummy semiconductor devices and dummy metal lines in the corner regions of said plurality of integrated circuits wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy semiconductor devices and an active area of a substrate of one of said plurality of integrated circuits; and

wherein said dummy metal lines prevent propagation of cracks in said corner regions of said integrated circuits.

2. The method according to claim 1 wherein said dummy metal lines comprise copper.

3. The method according to claim 1 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

4. The method according to claim 1 further comprising separating said plurality of integrated circuits from one another.

5. The method according to claim 4, wherein said separating step comprises wafer sawing or wafer dicing.

6. The method according to claim 1 wherein low dielectric constant dielectric material separates conducting layers from one another.

7. The method according to claim 1 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

8. The method according to claim 1 wherein said dummy metal lines comprise an alternating dummy grid structure.

9. The method according to claim 1 wherein said dummy metal lines comprise odd and even via stacks connected to alternate metal layers and wherein each of said alternate metal layers connects to either said odd via stacks or said even via stacks.

10. A method of fabricating an integrated circuit device comprising:

providing a plurality of integrated circuits on a wafer;

fabricating a dummy structure in a corner region of each of said plurality of integrated circuits comprising:

fabricating dummy polysilicon semiconductor devices and dummy metal

lines in the corner regions of said plurality of integrated circuits wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy polysilicon semiconductor devices and an active area of a silicon substrate of one of said plurality of integrated circuits; and

wherein said dummy metal lines prevent propagation of cracks in said corner regions of said integrated circuits.

11. The method according to claim 10 wherein said dummy metal lines comprise copper.

12. The method according to claim 10 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

13. The method according to claim 10 wherein low dielectric constant dielectric material separates conducting layers from one another.

14. The method according to claim 10 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

15. The method according to claim 10 further comprising separating said plurality of integrated circuits from one another.

16. The method according to claim 15, wherein said separating step comprises wafer sawing or wafer dicing.

17. The method according to claim 10 wherein said dummy metal lines comprise an alternating dummy grid structure.

18. The method according to claim 10 wherein said dummy metal lines comprise odd and even via stacks connected to alternate metal layers and wherein each of said alternate metal layers connects to either said odd via stacks or said even via stacks.

19. An integrated circuit comprising a dummy structure located at a corner region of said integrated circuit, said dummy structure comprising:

dummy semiconductor devices and dummy metal lines in the corner region of said integrated circuit wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy semiconductor device and an active area of a semiconductor substrate of said integrated circuit; and

wherein said dummy metal lines prevent propagation of cracks in said corner region of said integrated circuit.

20. The integrated circuit according to claim 19 wherein said dummy metal lines comprise copper.

21. The integrated circuit according to claim 19 wherein said metal layers and metal vias comprise copper, aluminum, or tungsten.

22. The integrated circuit according to claim 19 wherein delamination of metal layers during integrated circuit fabrication is also prevented by said dummy metal lines.

23. The integrated circuit according to claim 19 wherein said dummy metal lines comprise an alternating dummy grid structure.

24. The integrated circuit according to claim 19 wherein said dummy metal lines comprise odd and even via stacks connected to alternate metal layers.

25. The integrated circuit according to claim 24 wherein each of said alternate metal layers connects to either said odd via stacks or said even via stacks.

26. The integrated circuit according to claim 19, wherein low dielectric constant dielectric material separates conducting layers from one another.

27. An integrated circuit comprising a dummy structure located at a corner region of said integrated circuit, said dummy structure comprising:

dummy polysilicon semiconductor devices and dummy metal lines in a corner region of said integrated circuit wherein each of said dummy metal lines comprises a plurality of metal layers and wherein a lowest of said plurality of metal layers is connected by metal vias to both one of said dummy polysilicon semiconductor devices and an active area of a silicon substrate of said integrated circuit wherein said dummy metal lines prevent propagation of cracks in said corner region of said integrated circuit.