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INTEGRATED CIRCUIT DEVICE WITH COMPOSITE OXIDE DIELECTRIC

Related Application

This application is based upon prior filed copending provisional application No. 60/115,769 filed January 13, 1999.

Field of the Invention

The present invention relates to the field of integrated circuits, and, more particularly, to integrated circuit devices with a dielectric layer.

Background of the Invention

Typically, in a metal oxide semiconductor (MOS) transistor, a thin layer of silicon dioxide is grown in the gate region. The oxide functions as a dielectric whose thickness is chosen specifically to allow induction of a charge in the channel region under the oxide. The gate controls the flow of current through the device. In sub-0.5 m technologies, ultra-thin gate oxides are used for ultra-large-scale-integration (ULSI, more than 10 million transistors per chip).

Also, highly integrated memory devices, such as dynamic-random-access-memories (DRAMs), require a very thin dielectric film for the data storage capacitor. To meet this requirement, the capacitor dielectric film thickness will be below 2.5 nm of SiO_2 equivalent thickness. Use of a thin layer of a material having a higher relative permittivity, e.g. Ta_2O_5, in place of the conventional SiO_2 or Si_3N_4 layers is useful in achieving desired performance.

A chemical vapor deposited (CVD) Ta_2O_5 film can be used as a dielectric layer for this purpose, because the

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dielectric constant of Ta_2O_5 is approximately three times that of a conventional Si_3N_4 capacitor dielectric layer. However, one drawback associated with the Ta_2O_5 dielectric layer is undesired leakage current characteristics. Accordingly, although Ta_2O_5 material has inherently higher dielectric properties, Ta_2O_5 typically may produce poor results due to leakage current. For example, U.S. Patent No. 5,780,115 to Park et al., discloses the use of Ta_2O_5 as the dielectric for an integrated circuit capacitor with the electrode layer being formed of titanium nitride (TiN). However, at temperatures greater than 600 C, this layered structure has a stability problem because the titanium in the TiN layer tends to reduce the Ta_2O_5 of the dielectric layer into elemental tantalum.

Summary of the Invention

In view of the foregoing background, it is therefore an object of the invention to provide a low leakage, high quality gate or capacitor dielectric.

It is a further object of the invention to prevent the reduction of the dielectric by the metal of the conductor layer.

These and other objects, features and advantages in accordance with the present invention are provided by a semiconductor device including a first metal oxide layer, e.g. a tantalum oxide layer, adjacent a substrate, and a second metal oxide layer on the first metal oxide layer opposite the semiconductor substrate. A metal nitride layer, which includes a metal that may be capable of reducing the first metal oxide layer, is on the second metal oxide layer opposite the first metal oxide layer. The second metal oxide layer substantially blocks reduction of

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the first metal oxide layer by the metal of the metal nitride layer.

The first metal oxide layer may be tantalum pentoxide and the second metal oxide layer may preferably be titanium dioxide. Also, the second metal oxide layer may be zirconium dioxide, or ruthenium dioxide and preferably has a dielectric constant greater than about 25.

The substrate may comprise silicon and have a channel region therein beneath the first metal oxide layer to define a transistor in combination with the gate provided by the metal nitride layer. Furthermore, a silicon oxide layer between the substrate and the first metal oxide layer may be present and together with the substrate, may define an interface with respective substantially stress-free regions adjacent the interface. Alternatively, the device may include a conductive layer, e.g. a metal layer, between the substrate and the first metal oxide layer to define a capacitor with the metal nitride layer. Such a capacitor may include a silicon oxide layer between the conductive layer and the first metal oxide layer, and an insulating layer between the substrate and the conductive layer.

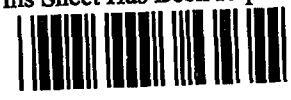
Brief Description of the Drawings

FIG. 1 is a schematic cross-sectional view of an integrated circuit device in accordance with the present invention;

FIG. 2 is a schematic cross-sectional view of a transistor in accordance with the present invention;

FIG. 3 is a schematic cross-sectional view of a capacitor in accordance with the present invention; and

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FIGS. 4-8 are schematic cross-sectional views of the steps in accordance with the fabrication method of the present invention.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

The basic layers of an integrated circuit device **9** according to the present invention will be described with reference to FIG. 1. The device **9** includes a substrate **10** which is made of silicon, for example. An insulation layer **13**, typically silicon dioxide, is disposed on the substrate **10**. Next, the device **9** includes a first metal oxide layer **15** and a second metal oxide layer **17** on the insulation layer **13**. The first metal oxide layer **15** can be formed of, for example, tantalum pentoxide (Ta_2O_5), while the second metal oxide layer **17** includes a metal oxide with a relatively high dielectric constant ( ), for example, greater than about 25. Such a high dielectric metal oxide preferably includes titanium dioxide (TiO_2), and also includes zirconium dioxide (ZrO_2) and ruthenium dioxide (RuO_2), for example. The first and second metal oxide layers form a high- composite dielectric stack **18**.

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The device 9 includes a metal nitride layer 19 on the second metal oxide layer 17. The metal nitride layer 19 may include titanium nitride (TiN) of which the titanium is capable of breaking down or reducing the metal oxide, e.g. tantalum pentoxide, of the first metal oxide layer 15 into, for example, elemental tantalum, as discussed above. However, the high dielectric second metal oxide layer 17 substantially blocks the breakdown or reduction of the metal oxide of the first metal oxide layer by the metal of the metal nitride layer 19. Thus, the device is stable at temperatures over 600 C and the use of the high- composite dielectric stack 18 allows scaling for sub-0.25 m devices without tunneling or breakdown.

Additionally, the device 9 may include a second silicon dioxide layer 11 to define an essentially planar and stress-free interface between the substrate 10 and the insulation layer 13. The interface traps defects resulting in the reduction of the defect densities of the insulation layer 13 and substrate 10.

A transistor 21 incorporating the high- composite dielectric stack of the present invention, as a gate dielectric, will be described with reference to FIG. 2. The transistor 21 includes a substrate 22 having a source 33, drain 35 and a channel region 37 therein, as would readily be appreciated by the skilled artisan. An insulation layer 23 is disposed above the channel region 37. The transistor includes a high- composite dielectric stack 31 made up of first and second metal oxide layers 25 and 27. Again, the first metal oxide layer 25 can be formed of Ta_2O_5, while the second metal oxide layer 27 includes a metal oxide with a relatively high dielectric constant such as TiO_2, ZrO_2 and RuO_2.

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The transistor 21 includes a metal nitride layer 29 on the second metal oxide layer 27. The metal nitride layer 29 may include TiN of which the titanium is capable of breaking down or reducing the metal oxide, e.g. tantalum pentoxide, of the first metal oxide layer 25 into, for example, elemental tantalum, as discussed above. However, the high dielectric second metal oxide layer 27 substantially blocks the breakdown or reduction of the metal oxide of the first metal oxide layer 25 by the metal of the metal nitride layer 29.

The transistor may also include an essentially planar and stress-free interface between the substrate 22 and the insulation layer 23. This interface would be formed as described below with reference to the device of FIG. 1.

Next, a metal-oxide-metal (MOM) capacitor 41 incorporating the high- composite dielectric stack of the present invention, as a capacitor dielectric, will be described with reference to FIG. 3. The capacitor 41 includes a substrate 42, a first insulation layer 51 and a first metal conductive layer 53, as would readily be appreciated by the skilled artisan. A second insulation layer 43 is disposed on the first conductive layer 53. The capacitor 41 includes a high- composite dielectric stack 55 made up of first and second metal oxide layers 45 and 47. Again, the first metal oxide layer 45 can be formed of Ta_2O_5, while the second metal oxide layer 47 includes a metal oxide with a relatively high dielectric constant such as TiO_2, ZrO_2 and RuO_2.

The capacitor 41 includes a second metal conductive layer 49 which includes a metal nitride, such as TiN, of which the titanium is capable of breaking down or reducing

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the metal oxide of the first metal oxide layer **45**, as discussed above. However, the high dielectric second metal oxide layer **47** substantially blocks the breakdown or reduction of the metal oxide of the first metal oxide layer **45** by the metal of the second conductive layer **49**.

A description of a method of fabricating an integrated device, such as the device **9** of FIG. 1, including a high- composite dielectric stack will be described with reference to FIGS. 4-8. As illustrated in FIG. 4, a silicon substrate **10** is provided and an insulation layer **13** is grown or deposited thereon. As discussed above, this insulation layer is typically SiO_2. Next, as shown in FIG. 5, a first metal oxide layer **15**, such as Ta_2O_5, is deposited using chemical vapor deposition techniques, for example. This is followed by the deposition of a second metal oxide layer **17** as illustrated in FIG. 6. As also discussed above, this second metal oxide layer **17** includes a metal oxide with a relatively high dielectric constant such as TiO_2, ZrO_2 and RuO_2. Again, such a metal oxide is preferably TiO_2.

The first and second metal oxide layers **15** and **17** make up the high- composite dielectric stack **18**. Furthermore, it is this high dielectric second metal oxide layer **17** which will substantially block the reduction of the metal oxide of the first metal oxide layer **15** by the metal of the subsequently deposited metal nitride layer **19**, shown in FIG. 8.

Additionally, as shown in FIG. 7, a second SiO_2 layer **11** may be grown before the metal nitride layer **19** is deposited. This second silicon dioxide layer **11** is grown by diffusing oxygen through the first and second metal oxide layers **15**, **17** and the insulation layer **13** during an anneal in an oxidizing atmosphere. Also, the growth of the second

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SiO_2 layer 11 occurs in near equilibrium condition and thus has excellent structural properties. This second SiO_2 layer 11 growth results in a stress-free and planar interface with desirable interfacial and electrical properties.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

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Claims:

1. A semiconductor device comprising:

a semiconductor substrate;

a tantalum oxide layer adjacent said substrate;

a metal oxide layer on said tantalum oxide layer opposite said semiconductor substrate; and

a metal nitride layer on said metal oxide layer opposite said tantalum oxide layer, said metal nitride layer comprising a metal capable of reducing said tantalum oxide layer;

said metal oxide layer substantially blocking reduction of said tantalum oxide layer by said metal of said metal nitride layer.

2. A semiconductor device according to Claim 1 wherein said tantalum oxide layer comprises tantalum pentoxide.

3. A semiconductor device according to Claim 1 wherein said metal oxide layer comprises titanium oxide.

4. A semiconductor device according to Claim 1 wherein said metal oxide layer comprises at least one of titanium oxide, zirconium oxide, and ruthenium oxide.

5. A semiconductor device according to Claim 1 wherein said metal nitride layer comprises titanium nitride.

6. A semiconductor device according to Claim 1 wherein said metal oxide layer has a dielectric constant greater than about 25.

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7. A semiconductor device according to Claim 1 wherein said substrate comprises silicon; and wherein said substrate has a channel region therein beneath said tantalum oxide layer.

8. A semiconductor device according to Claim 7 further comprising a silicon oxide layer between said substrate and said tantalum oxide layer.

9. A semiconductor device according to Claim 8 wherein said substrate and said silicon oxide layer define an interface; and wherein respective regions of said substrate and said silicon oxide layer adjacent said interface are substantially stress-free.

10. A semiconductor device according to Claim 1 further comprising a silicon oxide layer between said substrate and said tantalum oxide layer; wherein said substrate and said silicon oxide layer define an interface; and wherein respective regions of said substrate and said silicon oxide layer adjacent said interface are substantially stress-free.

11. A semiconductor device according to Claim 1 further comprising a conductive layer between said substrate and said tantalum oxide layer to define a capacitor with said metal nitride layer.

12. A semiconductor device according to Claim 11 wherein said conductive layer comprises a metal.

13. A semiconductor device according to Claim 11 further comprising a silicon oxide layer between said conductive layer and said tantalum oxide layer.

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14. A semiconductor device according to Claim 11 further comprising an insulating layer between said substrate and said conductive layer.

15. A semiconductor device comprising:

a semiconductor substrate;

a tantalum oxide layer adjacent said substrate;

a titanium oxide layer on said tantalum oxide layer and opposite said semiconductor substrate; and

a titanium nitride layer on said titanium oxide layer opposite said tantalum oxide layer.

16. A semiconductor device according to Claim 15 wherein said titanium oxide layer has a dielectric constant of about 25.

17. A semiconductor device according to Claim 15 wherein said substrate comprises silicon; and wherein said substrate has a channel region therein beneath said tantalum oxide layer.

18. A semiconductor device according to Claim 17 further comprising a silicon oxide layer between said substrate and said tantalum oxide layer.

19. A semiconductor device according to Claim 18 wherein said substrate and said silicon oxide layer define an interface; and wherein respective regions of said substrate and said silicon oxide layer adjacent said interface are substantially stress-free.

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20. A semiconductor device according to Claim 15 further comprising a silicon oxide layer between said substrate and said tantalum oxide layer; wherein said substrate and said silicon oxide layer define an interface; and wherein respective regions of said substrate and said silicon oxide layer adjacent said interface are substantially stress-free.

21. A semiconductor device according to Claim 15 further comprising a conductive layer between said substrate and said tantalum oxide layer to define a capacitor with said metal nitride layer.

22. A semiconductor device according to Claim 21 wherein said conductive layer comprises a metal.

23. A semiconductor device according to Claim 21 further comprising a silicon oxide layer between said conductive layer and said tantalum oxide layer.

24. A semiconductor device according to Claim 21 further comprising an insulating layer between said substrate and said conductive layer.

25. An integrated circuit device comprising:

a semiconductor substrate;

a first metal oxide layer adjacent said substrate, said first metal oxide layer including a metal oxide which is susceptible to reduction;

a second metal oxide layer on said dielectric oxide layer opposite said semiconductor substrate; and

a metal nitride layer on said second metal oxide layer opposite said first metal oxide layer, said metal

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nitride layer comprising a metal capable of reducing said metal oxide of said first metal oxide layer;

said second metal oxide layer substantially blocking reduction of said metal oxide by said metal of said metal nitride layer.

26. An integrated circuit device according to Claim 25 wherein said metal oxide of said first metal oxide layer comprises at least one of tantalum oxide and tantalum pentoxide.

27. An integrated circuit device according to Claim 25 wherein said second metal oxide layer comprises at least one of titanium oxide, zirconium oxide, and ruthenium oxide.

28. An integrated circuit device according to Claim 25 wherein said metal nitride layer comprises titanium nitride.

29. An integrated circuit device according to Claim 25 wherein said metal oxide layer has a dielectric constant greater than about 25.

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