

SPECIFICATION

Improvements in complex logic circuits

5 The present invention relates to improvements in a complex logic circuit composed of ECL (emitter coupled logic) circuitry. 5

An ECL (or often CML: current mode logic) circuit can be represented by one which consists of a differential transistor circuit only without an emitter follower output circuit as shown in Fig. 1 of the accompanying drawings, and by one which consists of a differential transistor circuit and an emitter follower output circuit as shown in Fig. 2 of the accompanying drawings. The ECL circuit without an emitter follower output circuit and the ECL circuit having an emitter follower output circuit, have been disclosed in the journal "CIRCUIT DESIGN FOR INTEGRATED ELECTRONICS" by H.R. Camenzind, published by Addison-Wesley Co., 1968, pp. 157-159. 10

The provision of the emitter follower output circuit presents certain advantages such as increased driving ability while enabling a wired-OR circuit to be constructed, but also presents certain disadvantages such as increased delay time (usually from 0.2 to 0.3 nanoseconds) due to the emitter follower circuit, increased power consumption, as well as increased number of elements for constituting the circuit. 15

When the emitter follower output circuit is eliminated, on the other hand, the circuit operates at high speeds whilst consuming less electric power. For relatively heavy loads having a large number of fan outs, however, the circuit cannot operate at high speeds since its driving ability is small, and it also becomes difficult to constitute wired-OR circuits. 20

In designing control logic circuits (random logic circuits) consisting of gate circuits, logic arithmetic circuits, shift registers, and the like, we have contrived to exploit the features of the above-mentioned two types of ECL circuits or to use the ECL circuit of either type depending on whether the load is heavy or light. The ECL circuit without the emitter follower output circuit shown in Fig. 1 is used for driving relatively light loads so that the operation can be carried out at high speeds under the light load conditions, whilst the ECL circuit having the emitter follower output circuit shown in Fig. 2 is used for driving relatively heavy loads of for performing the wired-OR function. 25

In the ECL circuit shown in Fig. 1, a reference voltage V_R is set to be, for example, -0.3 volts, the high level of the input voltage V_{IN} is set to be zero volts, and the low level of the input voltage V_{IN} is set to be about -0.6 volts. In the ECL circuit shown in Fig. 2, on the other hand, the reference voltage V_R is set to be -1.1 volts, the high level of the input voltage V_{IN} is set to be -0.8 volts, and the low level of the input voltage V_{IN} is set to be about -1.4 volts. However, when signals are to be delivered and received between the ECL circuit of Fig. 1 and the ECL circuit of Fig. 2, it becomes necessary to provide a level converting circuit. The use of a level converting circuit has the following disadvantages: 30

- (a) it is difficult to maintain highspeed operation;
- (b) it is difficult to simplify the circuit setup; and
- (c) it is difficult to reduce the consumption of electric power. Furthermore, in designing the logic circuits, the difference in the signal levels must be taken into consideration; i.e. the level converting circuit makes the design complicated. Moreover, it is necessary to provide two circuits for generating the reference voltage V_R . 35

From the above noted difficulties, it was obvious that a complex logic circuit made up of the combination of the ECL circuit Fig. 1 and the ECL circuit of Fig. 2, was less efficient than a complex logic circuit constructed by using the ECL circuit of Fig. 1 alone or by using the ECL circuit of Fig. 2 alone in the known manner. 40

It is an object of the present invention to overcome the above disadvantages by providing a complex logic circuit which operates at high speeds, which consumes less electric power, and which enables the circuit setup to be simplified. 45

According to the present invention, there is provided a complex logic circuit including:

- (a) a first emitter coupled logic circuit without an emitter follower output circuit; and
 - (b) a second emitter coupled logic circuit having an emitter follower output circuit;
- wherein level shift means is connected between a load resistor of said first emitter coupled logic circuit and a point of operation potential, and the voltage drop across said level shift means is set to be substantially equal to a voltage across the base and emitter electrodes of the emitter follower output transistor of said emitter follower output circuit of said second emitter coupled logic circuit. 50

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein: 55

Figure 3 is a block diagram of a full-adder circuit which constitutes a portion of a complex logic circuit to which a first embodiment of the present invention is applied;

Figure 4 is a block diagram of a signal gate circuit which constitutes a portion of a complex logic circuit to which the first embodiment is applied; 60

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Figure 5 is a circuit diagram showing a part of the block diagram shown in Fig. 3, and constituting the first embodiment;

Figure 6 is a block diagram of a latch circuit which constitutes a portion of a complex logic circuit to which the first embodiment is applied;

5 Figure 7 is a circuit diagram of a wired-OR setup which constitutes a portion of a complex logic circuit; to which the first embodiment is applied;

Figure 8 is a circuit diagram according to a second embodiment of part of a complex logic circuit;

10 Figure 9 is a circuit diagram of a fundamental circuit setup for forming part of a complex logic circuit relying upon a monolithic semiconductor integrated circuit of the master slice type; and

Figure 10 is a circuit diagram in which that part of the fundamental circuit setup of Fig. 9 is not provided with an emitter follower output circuit.

The full adder circuit shown in Fig. 3 has been widely used for adding binary digits, and comprises an inverter circuit IN1 to the input terminal of which is applied an input signal X; an inverter circuit IN2 to the input terminal of which is applied an input signal Y; and an inverter circuit IN3 to the input terminal of which is applied a carry input signal C1. Inverted signals $\bar{X}$, $\bar{Y}$ and $\bar{C1}$ are output from the respective inverters IN1, IN2 and IN3. The full adder circuit also comprises NOR gate circuits G1 to G7 to the inputs of which are applied the input signals X, Y and C1 and the inverted signals thereof $\bar{X}$, $\bar{Y}$ and $\bar{C1}$; an OR gate circuit G8 to the inputs of which are applied the output signals of NOR gate circuits G1 to G4; and an OR gate circuit G9 to the inputs of which are applied the output signals of NOR gate circuits G5 to G7.

An output signal S from the OR gate circuit G8 is given by the following logic equation:

$$25 \quad S = \bar{X} + \bar{Y} \bar{C1} + X + \bar{Y} + C1 + X + Y + \bar{C1} + \bar{X} + Y + C1 \quad (1) \quad 25$$

A carry output signal C2 from the OR gate circuit G9 is given by the following logic equation:

$$30 \quad C2 = \bar{X} + \bar{Y} + \bar{X} + \bar{C1} + \bar{Y} + \bar{C1} \quad (2) \quad 30$$

The full adder circuit can be constituted by ECL circuits. In this embodiment ECL circuits having an emitter follower output circuit are used as the inverter circuits IN1 to IN3 with many fan outs, and ECL circuits which have level shift means between a collector load resistor and a predetermined voltage terminal, and which consist of a differential transistor circuit only having a signal level which is in agreement with the signal level of the ECL circuits having an emitter follower output circuit, are used as NOR gate circuits G1 to G7 having one fan out.

This is illustrated in further detail with reference to a preferred embodiment shown in Fig. 5.

40 For instance, the above-mentioned inverter circuit IN1 consists of a differential transistor circuit which includes a transistor Q12 the base electrode of which is connected to a terminal T4, a transistor Q11 the base electrode of which is connected to a terminal T3; a constant-current supply I_0 connected between a terminal T2 and the emitter electrodes of the transistors Q11 and Q12 which are connected in common; load resistors R11 and R12 connected between the collector electrodes of the respective transistors Q11 and Q12 and a terminal T1. The inverter circuit IN1 also includes an emitter follower output circuit which consists of a transistor Q13 the base electrode of which is connected to the collector electrode of the transistor Q11 and the collector electrode of which is connected to the terminal T1, and a resistor R13 which is connected between the emitter electrode of the transistor Q13 and the terminal T2.

50 A voltage of zero volts is applied to the terminal T1, a power-supply of negative voltage $-V_{EE}$ (-5.2 volts) is applied to the terminal T2, a reference voltage V_s of, for example, -1.3 V is applied to the terminal T4, and an input signal X is applied to the terminal T3.

The NOR gate circuit G1 includes: a transistor Q17, the base electrode of which is connected to the terminal T4; a transistor Q14 the base electrode of which is connected to the emitter electrode of the transistor Q13 which acts as an output terminal of the inverter circuit IN1; transistors Q15 and Q16 the base electrodes of which are connected to similar output terminals of other inverter circuits IN2 and IN3; a constant-current supply circuit $10'$ which is connected between the terminal T2 and the emitter electrodes of the transistors Q14 to Q17 which are all connected in common; a collector load resistor R15 one end of which is connected to the collector electrode of the transistor Q17; a collector load resistor R14 one end of which is connected to the collector electrodes of the transistors Q14 to Q16 in common; and a transistor Q18 which is connected in the manner of a diode between the other ends of the resistors R14 and R15 and the terminal T1. The transistor Q18 which acts as a diode serves as a level shift means. In an alternative form the transistor Q18 can be replaced by a diode. Output signals are obtained from the collector electrodes of the transistors Q14 to Q16 which are connected in

common.

The other two inverter circuits IN2 and IN3 of Fig. 3 are also constructed in similar manner to the inverter circuit IN1 of Fig. 5, and the other six NOR gate circuits G2 to G7 of Fig. 3 are also constructed in similar manner to the NOR gate circuit G1 of Fig. 5.

5 When there is only one fan out, the OR gate circuits G8 and G9 of Fig. 3 are constructed in similar manner to the gate circuit G1 of Fig. 5. However, since they are OR gate circuits, the output signal S or C2 is obtained from the collector electrode of a transistor which is supplied with the reference voltage V_s through its base electrode. On the other hand, when there are many fan outs, the ECL circuit having the emitter follower output circuit is used like the inverter circuit IN1 of Fig. 5. However, since many input signals exist, the corresponding number of transistors have to be arrayed in parallel. Furthermore, since the OR gate circuit is employed, the output signal S or C2 is obtained from the emitter follower output circuit to whose base electrode is connected the collector electrode of the transistor that is supplied with the reference voltage V_s through its base electrode.

10 Referring to the NOR gate circuit G1 in the circuit of Fig. 5, a voltage of zero volts of which the level is shifted, is applied to the collector resistors R14 and R15 relying upon a voltage V_{BE} across the base and emitter electrodes of the transistor Q18. Therefore, the high level can be set to be about -0.7 volts. The signal level between the two circuits can be set to be nearly equal by employing the collector resistors R14 and R15 and the constant-current circuit 10' having resistances and current values which are the same as those of the collector resistances R12 and R13 and constant-current circuit 10 of the inverter circuit IN1. As illustrated in Fig. 5, the reference voltage V_s can be commonly utilized, and the inverter circuit IN1 and the NOR gate circuit which are the two ECL circuits having different circuit types can be directly connected together without the need of providing a level converting circuit.

15 Fig. 4 is a circuit diagram illustrating the application of the first embodiment to a signal gate circuit which constitutes a portion of a complex logic circuit. The circuit consists of OR gate circuits G10 to G14 to the first input terminals of which are applied signals A to E, and an inverter circuit IN4 to the input of which is applied a gate control signal ϕ . The output signal of the inverter circuit IN4 is applied in common to the second input terminals of the OR gate circuits G10 to G14.

20 When the gate control signal ϕ has the level "0", an inverted output signal $\bar{\phi}$ thereof has the level "1", whereby the output signal A' to E' of the OR gate circuits G10 to G14 assume the level "1" irrespective of the input signals A to E. On the other hand, when the gate control signal ϕ has the level "1", the inverted output signal $\bar{\phi}$ thereof has the level "0", and the output signals A' to E' of the OR gate circuits G10 to G14 assume the levels which correspond to the input signals A to E.

25 When the individual OR gate circuits G10 to G14 have only one fan out, the signal gate circuit employs, as OR gate circuits G10 to G14, the ECL circuits which have level shift means between the collector load resistor and a predetermined voltage terminal as illustrated with reference to the gate circuit G1 of Fig. 5, but which do not have the emitter follower output circuit. On the other hand, since the inverter circuit IN4 has a large number of fan outs, the ECL circuit having the emitter follower output circuit is used as illustrated with reference to the inverter circuit IN1 of Fig. 5.

30 Fig. 6 is a circuit diagram illustrating the application of the first embodiment to a latch circuit which constitutes a portion of a complex logic circuit. The circuit includes four flip-flop circuits FF1 to FF4 and an inverter IN5. A timing signal ϕ_2 is applied, via the inverter circuit IN5, to the clock input terminals of the flip-flop circuits FF1 to FF4. Signals D1 to D4 are fed in synchronism with the inverted signal $\bar{\phi}_2$ to the respective flip-flop circuits FF1 to FF4.

35 The inverter circuit IN5 employs the ECL circuit having the emitter follower output circuit depending upon the number of fan outs, and the circuits constituting the flip-flop circuits FF1 to FF4 with a single fan out, are constructed of ECL circuits without an emitter follower output circuit but having the level shift means referred to above. The circuits having an increased number of fan outs are constructed by ECL circuits having an emitter follower output circuit.

40 The above description has dealt with the case where the two types of ECL circuits are selectively used depending upon the number of fan outs. Referring to Fig. 7, when a wired-OR circuit is to be constructed by directly connecting the outputs of NOR gate circuits G15 to G17, the ECL circuit having an emitter follower output circuit is employed irrespective of the number of fan outs. In this case, the emitter electrodes of the output transistors of the emitter follower output circuits constituting NOR gate circuits, are connected in common to the common load resistors.

45 Fig. 8 is a circuit diagram illustrating a second embodiment of part of a complex logic circuit. The ECL circuit shown in Fig. 8 does not have an emitter follower output circuit but has level shift means consisting of a resistor R24 instead of level shift means consisting of a diode connected transistor Q18 which is shown in Fig. 5.

50 The circuit shown in Fig. 8 includes: a transistor Q22 the base electrode of which is

connected to a terminal T4; a transistor Q21 the base electrode of which is connected to the terminal T3; a transistor Q23 the collector electrode of which is connected to the emitter electrodes of the transistors Q21 and Q22 which are connected in common, and the base electrode of which is connected to a terminal T7; a resistor R23 connected between the emitter electrode of the transistor Q23 and a terminal T2; collector load resistors R21 and R22 connected to the collector electrodes of the transistors Q21 and Q22; and a level shift resistor R24 connected between a terminal T1 and the other ends of the collector load resistors R21 and R22 which are connected in common.

A voltage of zero volts is applied to the terminal T1 on the positive side and a negative voltage $-V_{EE}$ of, for example, -5.2 volts is applied to the terminal T2 on the negative side. A constant voltage V_{CS} is applied to the terminal T7, and a constant-current circuit is formed by the transistor Q23 and the emitter resistor R23. Furthermore, a reference voltage V_B is applied to the terminal T4, and a logic input signal IN is applied to the terminal T3. An inverted output signal $\overline{OUT}$ is obtained from the terminal T5 which is connected to the collector electrode of the transistor Q21, and a non-inverted output signal OUT is obtained from the terminal T6 which is connected to the collector electrode of the transistor Q22.

A constant current I_0 which is produced by the constant-current circuit is given by the following equation:

$$I_0 = (V_{CS} - V_{BEQ23})/R23 \quad (3)$$

Therefore, the voltage drop V through the level shift resistor R24 can be found from the following equation:

$$V = I_0 R24 = (V_{CS} - V_{BEQ23}) \frac{R24}{R23} \quad (4)$$

In these two equations the voltage V_{CS} and the voltage V_{BEQ23} across the base and emitter electrodes of the transistor Q23 remain constant. Accordingly, the voltage V is determined by the ratio of the resistance of the resistor R24 to resistance of the resistor R23. Even when the circuit of this second embodiment is constituted by a monolithic semiconductor integrated circuit, the resistance ratio can be precisely set in the monolithic semiconductor integrated circuit. Accordingly, the level shift means can be set up relying upon the resistances. Furthermore, by setting the voltage V to be equal to the voltage V_{BE} across the base and emitter electrodes of the transistor, the signal level can be brought into agreement with that of the ECL circuit having an emitter follower output circuit.

Fig. 9 is a circuit diagram of a fundamental circuit setup when part of the complex logic circuit is constructed in the form of a monolithic semiconductor integrated circuit relying upon the master slice system. The ECL circuit having an emitter follower circuit is provided with transistors Q31 to Q36, resistors R31 to R34, and a constant-current circuit I_0 . When the ECL circuit having an emitter follower output circuit is to be formed, connections are formed as indicated by dotted lines in Fig. 9. When that part of the ECL circuit without an emitter follower output circuit is to be formed, the connections are made as indicated by solid lines in Fig. 10. In this form, the ECL circuit is made up of the constant-current circuit I_0 , transistors Q31 to Q34, and resistors R31 and R32. Furthermore, the transistor Q36 which had been formed to constitute the emitter follower output circuit is connected in the manner of a diode between the resistors R31 and R32 and the terminal T1 which supplies the voltage.

When a resistor is to be used as the level shift means, the emitter resistor R34 which constitutes the emitter follower output circuit may be used.

In this case, it is necessary to set the resistance of the resistor R34 beforehand in such a manner that the above-mentioned resistance ratio is obtained depending upon the constant voltage V_{CS} of the constant-current circuit.

In constituting the complex logic circuit, the ECL circuit of relatively light loads is formed by that one not having an emitter follower output circuit, and the signal level is brought by the level shift means into agreement with that of the ECL circuit having an emitter follower output circuit, in such a manner that the signals can be directly delivered and received. Accordingly, the complex logic circuit features high-speed operation using an ECL circuit without an emitter follower output circuit under light load conditions. Furthermore, owing to the use of the ECL circuit without an emitter follower output circuit, the number of elements constituting the circuit can be reduced, and the consumption of electric current can also be reduced. Furthermore, when the complex logic circuit is to be formed in the form of a monolithic semiconductor integrated circuit, the degree of integration can be increased owing to the reduction in the number of elements. In particular, when the master slice system is employed, the ECL circuits of two different types can be selectively obtained based upon the same fundamental circuit setup.

A number of modifications to the embodiments described above are possible. For example, the signal levels and the voltages may be set to slightly different values. Furthermore, in order to reduce the consumption of electric power of the emitter follower output circuit, a terminal may be provided to supply a voltage which is lower than the low level, or to supply a voltage of

5 - 2 volts, and the load resistors of the emitter follower output circuit may be connected thereto. 5

Moreover, the ECL circuit having an emitter follower output circuit is better employed not only when there are many fan outs and the wired-OR function is to be performed, but also when the output wiring has large capacity although the number of fan outs is only one.

Thus, whether the ECL circuit having an emitter follower output circuit should be employed or 10 not, is determined depending upon whether the load carried by the ECL circuit without the emitter follower output circuit causes the signal delay time to become greater than the delay time in the emitter follower output circuit. 10

Furthermore, the differential transistor circuits constituting the ECL circuit having an emitter follower output circuit and the ECL circuit not having an emitter follower output circuit, may 15 have collector load resistors and the constant-current supplies having different values within such ranges that the signal levels of the two circuits are in agreement with each other. 15

CLAIMS

1. A complex logic circuit including:
20 (a) a first emitter coupled logic circuit without an emitter follower output circuit; and 20
(b) a second emitter coupled logic circuit having an emitter follower output circuit;

wherein level shift means is connected between a load resistor of said first emitter coupled logic circuit and a point of operation potential, and the voltage drop across said level shift means is set to be substantially equal to a voltage across the base and emitter electrodes of the 25 emitter follower output transistor of said emitter follower output circuit of said second emitter coupled logic circuit. 25

2. A complex logic circuit according to Claim 1, wherein said first emitter coupled logic circuit and said second emitter coupled logic circuit are formed in a monolithic semiconductor integrated circuit.

3. A complex logic circuit according to Claim 2, wherein a portion and other portions of a 30 group of fundamental circuit setups which are formed beforehand in the monolithic semiconductor integrated circuit are selectively connected in the configuration of said first emitter coupled logic circuit and in the configuration of said second emitter coupled logic circuit by the connection technique based upon the master slice system. 30

4. A complex logic circuit according to Claim 1, wherein said level shift means is a diode. 35

5. A complex logic circuit according to Claim 4, wherein said diode is constituted by a transistor connected to act as a diode.

6. A complex logic circuit according to Claim 1, wherein said level shift means is a resistor.

7. A complex logic circuit according to Claim 1, wherein said first emitter coupled circuit is a 40 NOR gate circuit and said second emitter coupled is an inverter. 40

8. A complex logic circuit according to Claim 7, wherein said circuit is formed to constitute an adder circuit, there being n inverters having a plurality of fan outputs, and $2n + 1$ NOR gates, and wherein a first OR gate receives the outputs from $n + 1$ NOR gates to provide an output signal, and a second OR gate receives the outputs from the other NOR gates to provide a 45 carry output signal. 45

9. A complex logic circuit according to Claim 1 designed as a signal gate circuit, wherein said first emitter coupled circuit comprises n OR gates, each receiving different input signals on a first input terminal, and said second emitter coupled circuit comprises an inverter which receives a gate control signal on its input, and which outputs an inverted signal to the second 50 inputs of the n OR gates. 50

10. A complex logic circuit according to Claim 1 designed as a latch circuit, wherein said first emitter coupled circuit comprises n flip-flops, each receiving different input signals on an input terminal, and said second emitter coupled circuit comprises an inverter which receives a clock pulse signal on its input, and which outputs an inverted signal to the clock inputs of the n 55 flip-flops. 55

11. A complex logic circuit according to Claim 1 designed as a wired-OR circuit, wherein said first emitter coupled circuit comprises an inverter and said second emitter coupled circuit is constituted by n NOR gates.

12. A complex logic circuit constructed substantially as herein described with reference to 60 Figs. 3 and 5; or any one of Figs. 4, 6 and 7 as adapted from the circuits shown in Fig. 5; or Fig. 5 having a part of the circuit modified by any one of Figs. 8, 9 and 10. 60



A number of modifications to the embodiments described above are possible. For example, the signal levels and the voltages may be set to slightly different values. Furthermore, in order to reduce the consumption of electric power of the emitter follower output circuit, a terminal may be provided to supply a voltage which is lower than the low level, or to supply a voltage of

5 - 2 volts, and the load resistors of the emitter follower output circuit may be connected thereto. 5

Moreover, the ECL circuit having an emitter follower output circuit is better employed not only when there are many fan outs and the wired-OR function is to be performed, but also when the output wiring has large capacity although the number of fan outs is only one.

Thus, whether the ECL circuit having an emitter follower output circuit should be employed or 10 not, is determined depending upon whether the load carried by the ECL circuit without the emitter follower output circuit causes the signal delay time to become greater than the delay time in the emitter follower output circuit. 10

Furthermore, the differential transistor circuits constituting the ECL circuit having an emitter follower output circuit and the ECL circuit not having an emitter follower output circuit, may 15 have collector load resistors and the constant-current supplies having different values within such ranges that the signal levels of the two circuits are in agreement with each other. 15

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2. A complex logic circuit according to Claim 1, wherein said first emitter coupled logic circuit and said second emitter coupled logic circuit are formed in a monolithic semiconductor integrated circuit.

30 3. A complex logic circuit according to Claim 2, wherein a portion and other portions of a group of fundamental circuit setups which are formed beforehand in the monolithic semiconductor integrated circuit are selectively connected in the configuration of said first emitter coupled logic circuit and in the configuration of said second emitter coupled logic circuit by the connection technique based upon the master slice system. 30

35 4. A complex logic circuit according to Claim 1, wherein said level shift means is a diode. 35

5. A complex logic circuit according to Claim 4, wherein said diode is constituted by a transistor connected to act as a diode.

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10. A complex logic circuit according to Claim 1 designed as a latch circuit, wherein said first emitter coupled circuit comprises n flip-flops, each receiving different input signals on an input terminal, and said second emitter coupled circuit comprises an inverter which receives a clock pulse signal on its input, and which outputs an inverted signal to the clock inputs of the n 55 flip-flops. 55

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12. A complex logic circuit constructed substantially as herein described with reference to 60 Figs. 3 and 5; or any one of Figs. 4, 6 and 7 as adapted from the circuits shown in Fig. 5; or Fig. 5 having a part of the circuit modified by any one of Figs. 8, 9 and 10. 60