ABSTRACT OF THE DISCLOSURE

Method for Transistor Fabrication with Optimized Performance

[039] A semiconductor process and apparatus includes forming <100> channel orientation CMOS transistors **(24, 34)** with enhanced hole mobility in the NMOS channel region and reduced channel defectivity in the PMOS region by depositing a first tensile etch stop layer **(51)** over the PMOS and NMOS gate structures, etching the tensile etch stop layer **(51)** to form tensile sidewall spacers **(62)** on the exposed gate sidewalls, and then depositing a second hydrogen rich compressive or neutral etch stop layer **(72)** over the NMOS and PMOS gate structures **(26, 36)** and the tensile sidewall spacers **(62)**. In other embodiments, a first hydrogen-rich etch stop layer **(81)** is deposited and etched to form sidewall spacers **(92)** on the exposed gate sidewalls, and then a second tensile etch stop layer **(94)** is deposited over the NMOS and PMOS gate structures **(26, 36)** and the sidewall spacers **(92)**.

Fig. 10