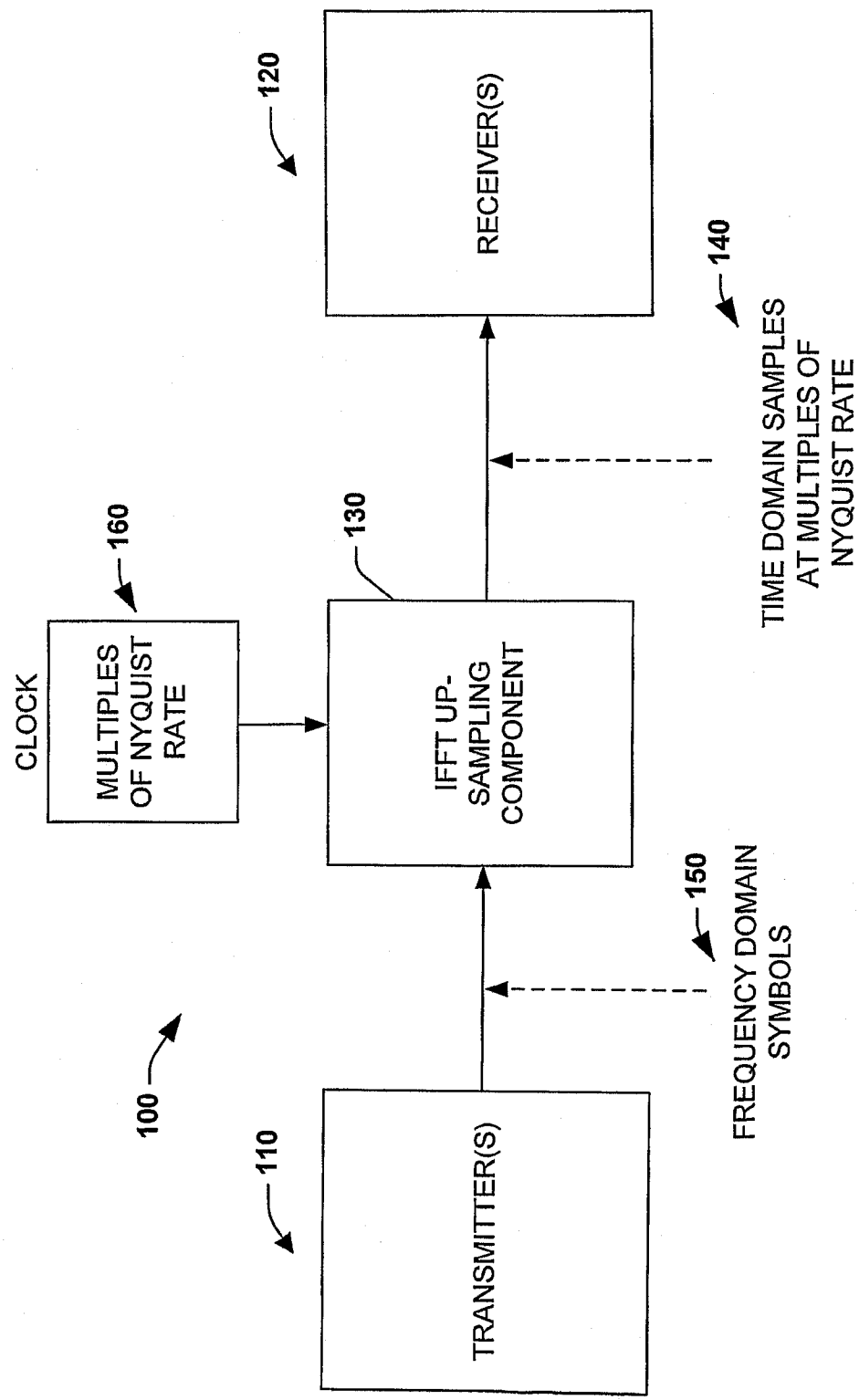

100
110
TRANSMITTER(S)
120
RECEIVER(S)
130
IFFT UP-SAMPLING COMPONENT
140
TIME DOMAIN SAMPLES AT MULTIPLES OF NYQUIST RATE
150
FREQUENCY DOMAIN SYMBOLS
160
CLOCK
MULTIPLES OF NYQUIST RATE

FIG. 1

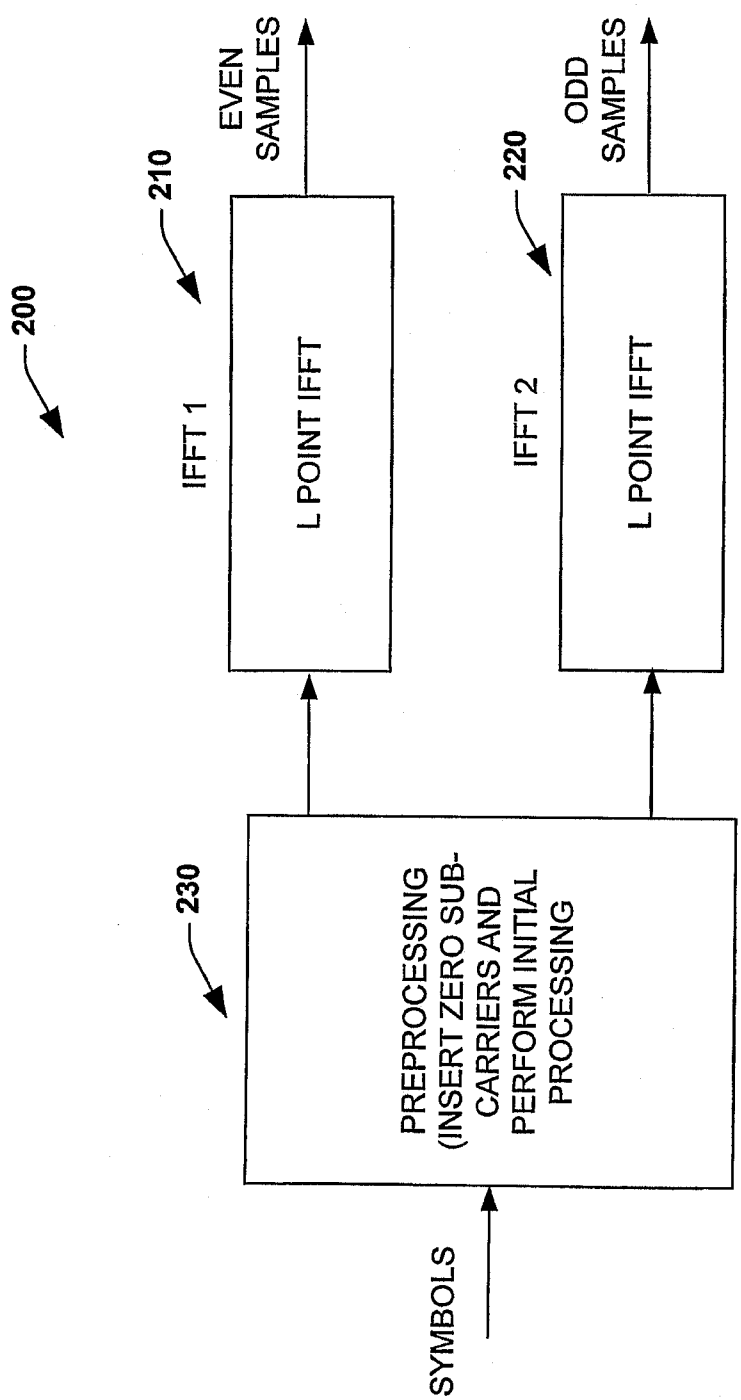

200
210
IFFT 1
L POINT IFFT
EVEN SAMPLES
220
IFFT 2
L POINT IFFT
ODD SAMPLES
230
PREPROCESSING (INSERT ZERO SUB-CARRIERS AND PERFORM INITIAL PROCESSING
SYMBOLS

FIG. 2

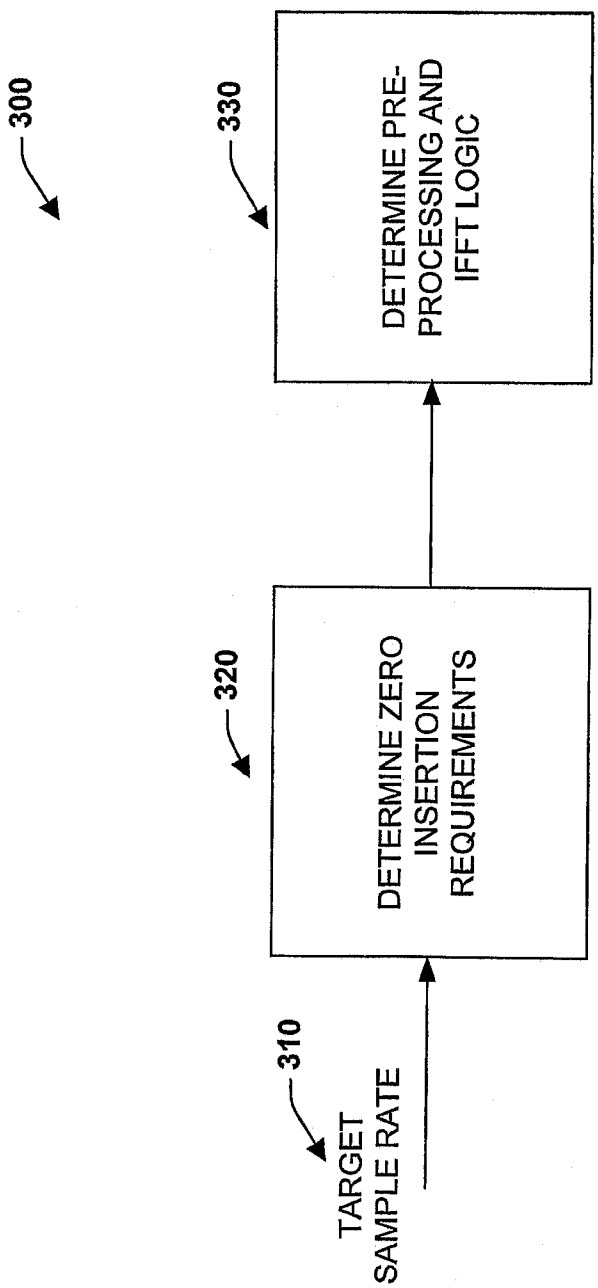

300
330
DETERMINE PRE-PROCESSING AND IFFT LOGIC
320
DETERMINE ZERO INSERTION REQUIREMENTS
310
TARGET SAMPLE RATE

FIG. 3

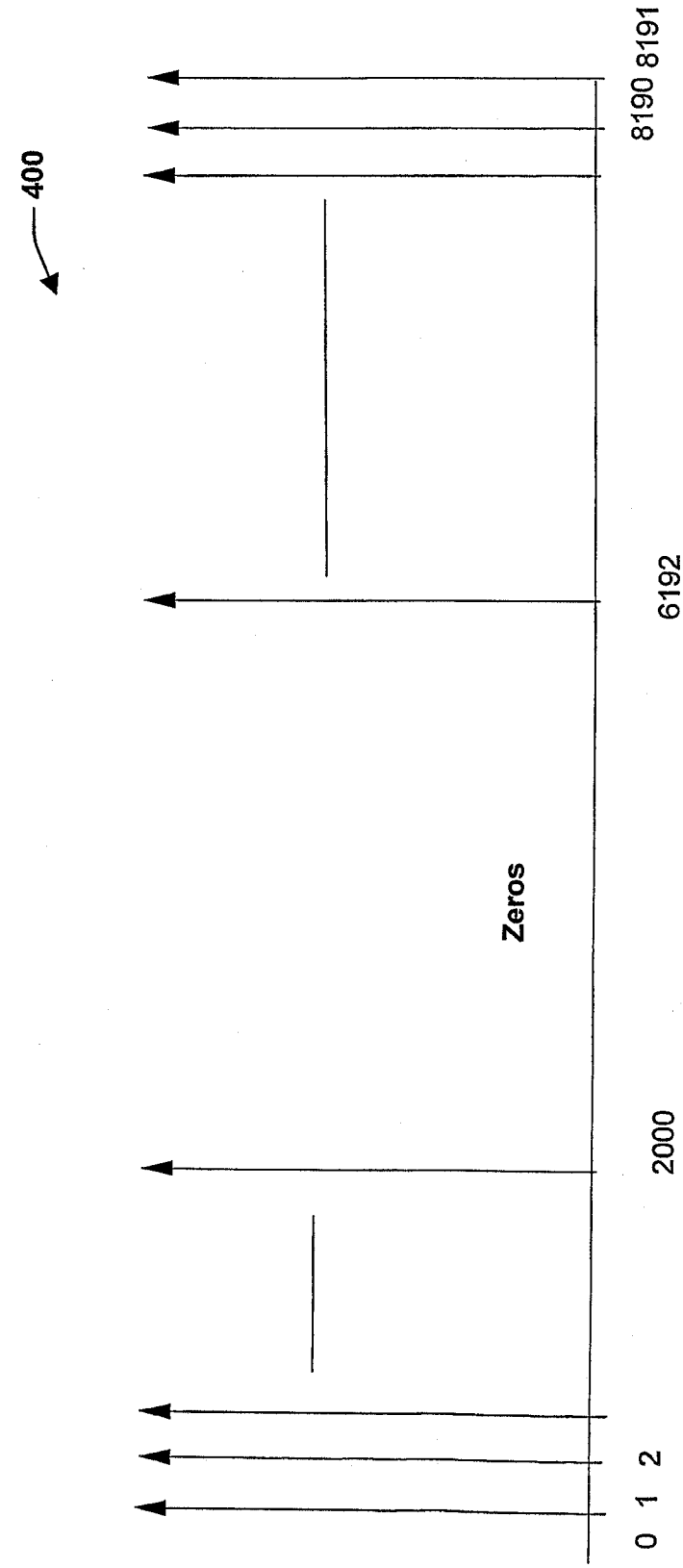


FIG. 4

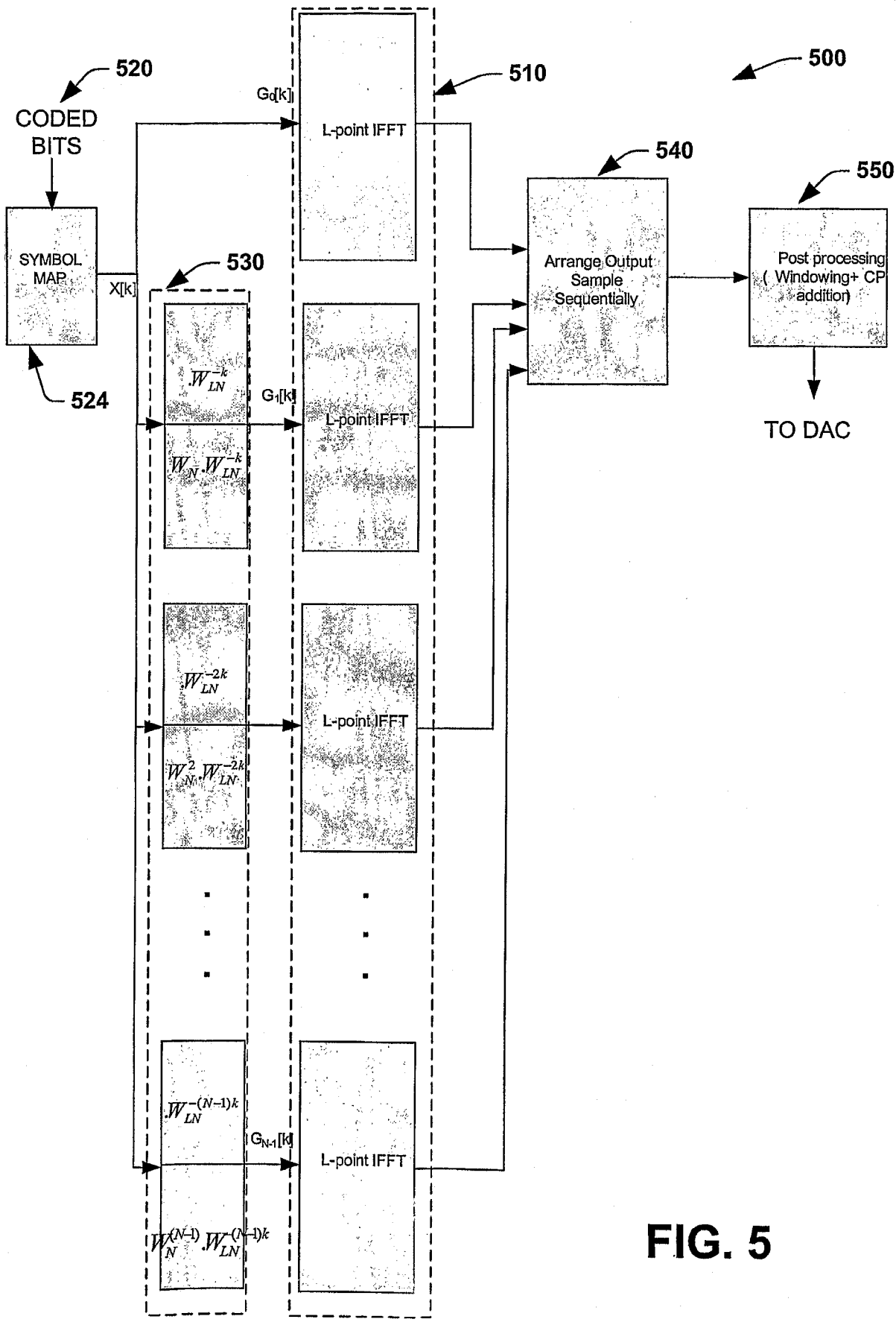

520
CODED BITS
SYMBOL MAP
524
X[k]
530
510
500
G0[k]
L-point IFFT
540
550
Arrange Output Sample Sequentially
Post processing (Windowing+ CP addition)
TO DAC
G1[k]
L-point IFFT
L-point IFFT
GN-1[k]
L-point IFFT

FIG. 5

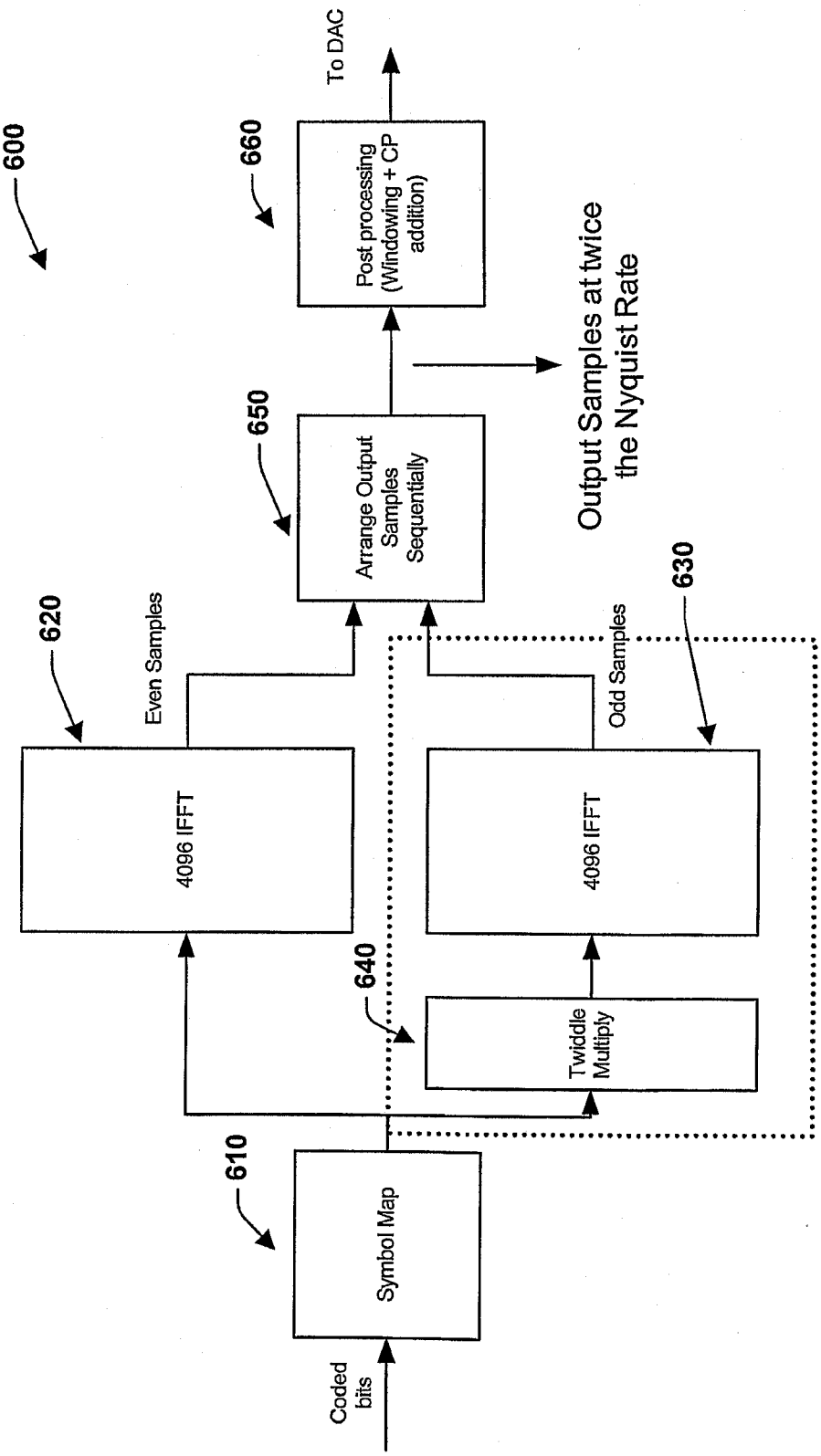

600
610
Symbol Map
Coded bits
620
4096 IFFT
Even Samples
630
4096 IFFT
Odd Samples
640
Twiddle Multiply
650
Arrange Output Samples Sequentially
Output Samples at twice the Nyquist Rate
660
Post processing (Windowing + CP addition)
To DAC

FIG. 6

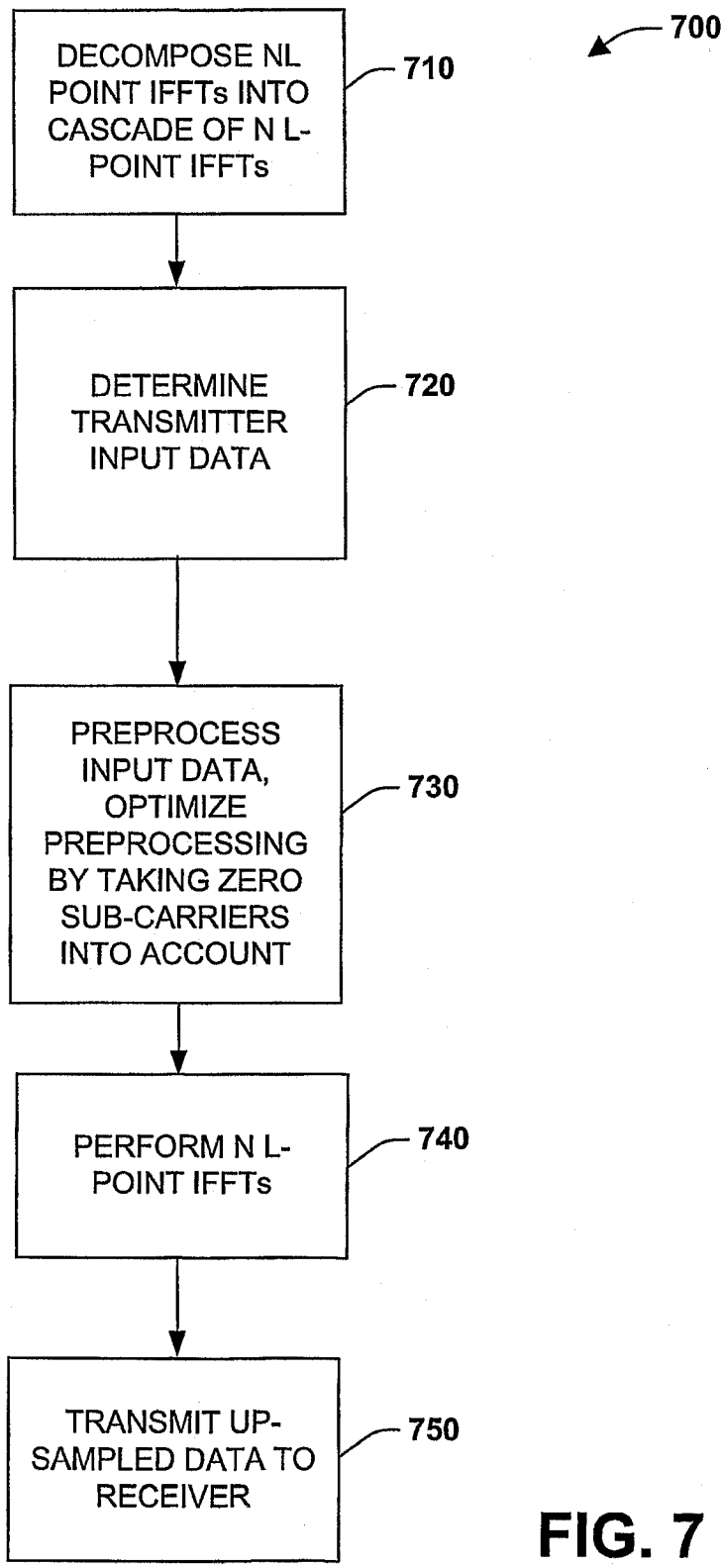

700
DECOMPOSE NL POINT IFFTs INTO CASCADE OF N L-POINT IFFTs
710
DETERMINE TRANSMITTER INPUT DATA
720
PREPROCESS INPUT DATA, OPTIMIZE PREPROCESSING BY TAKING ZERO SUB-CARRIERS INTO ACCOUNT
730
PERFORM N L-POINT IFFTs
740
TRANSMIT UP-SAMPLED DATA TO RECEIVER
750

FIG. 7

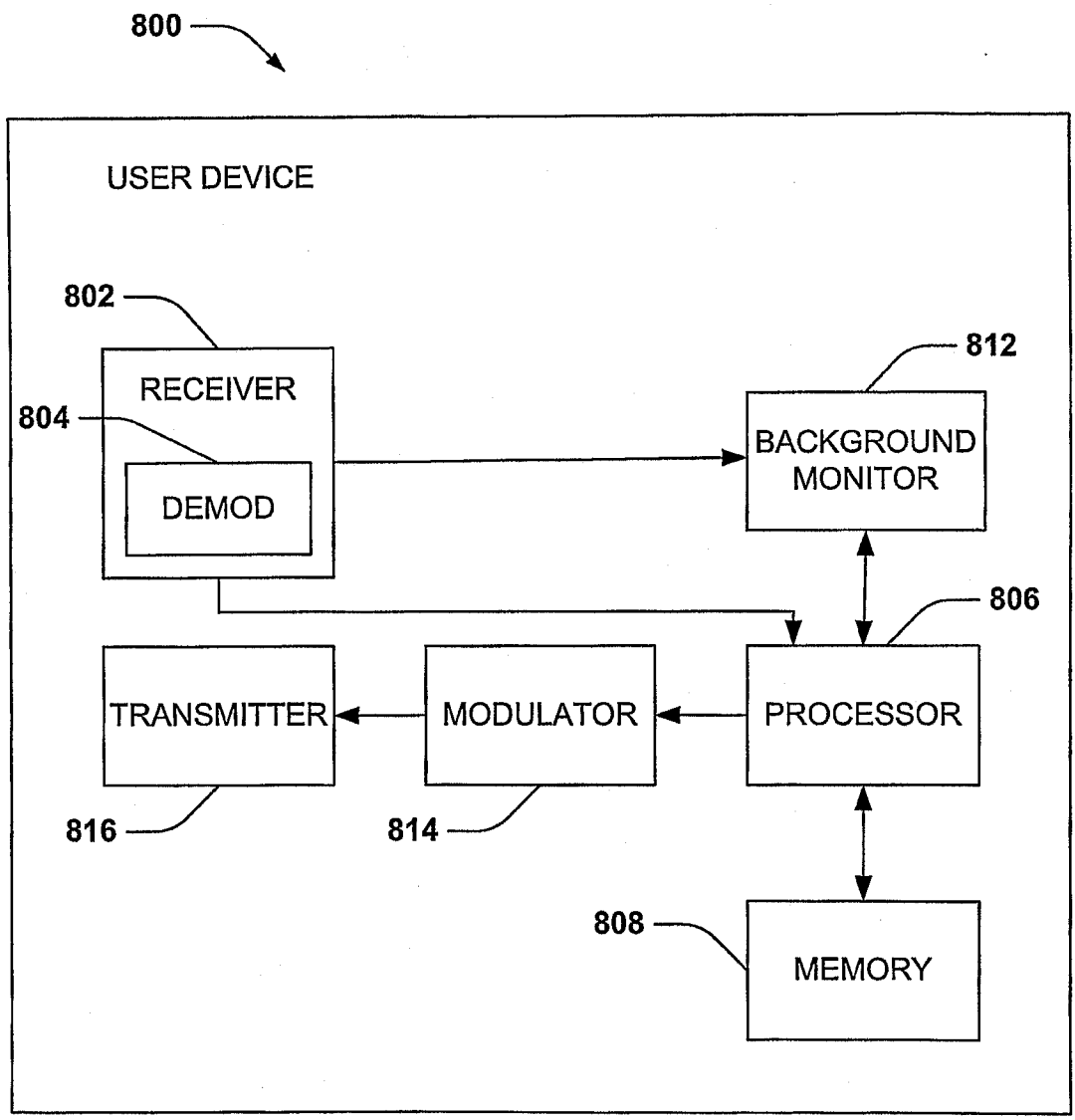

800
USER DEVICE
802
RECEIVER
804
DEMOD
812
BACKGROUND MONITOR
806
TRANSMITTER
MODULATOR
PROCESSOR
816
814
808
MEMORY

FIG. 8

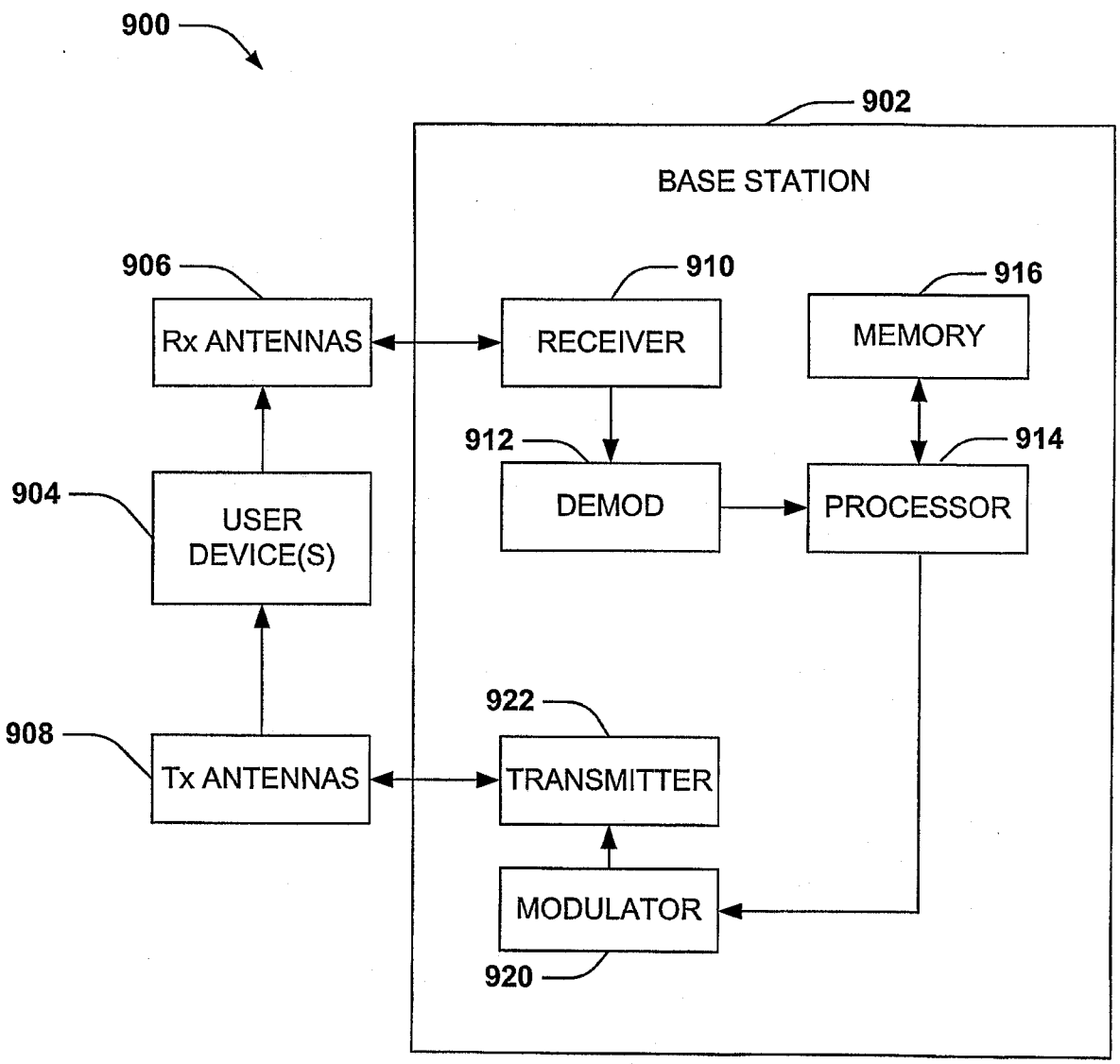

900
902
BASE STATION
906
Rx ANTENNAS
910
RECEIVER
916
MEMORY
912
DEMOD
914
PROCESSOR
904
USER
DEVICE(S)
908
Tx ANTENNAS
922
TRANSMITTER
MODULATOR
920

FIG. 9

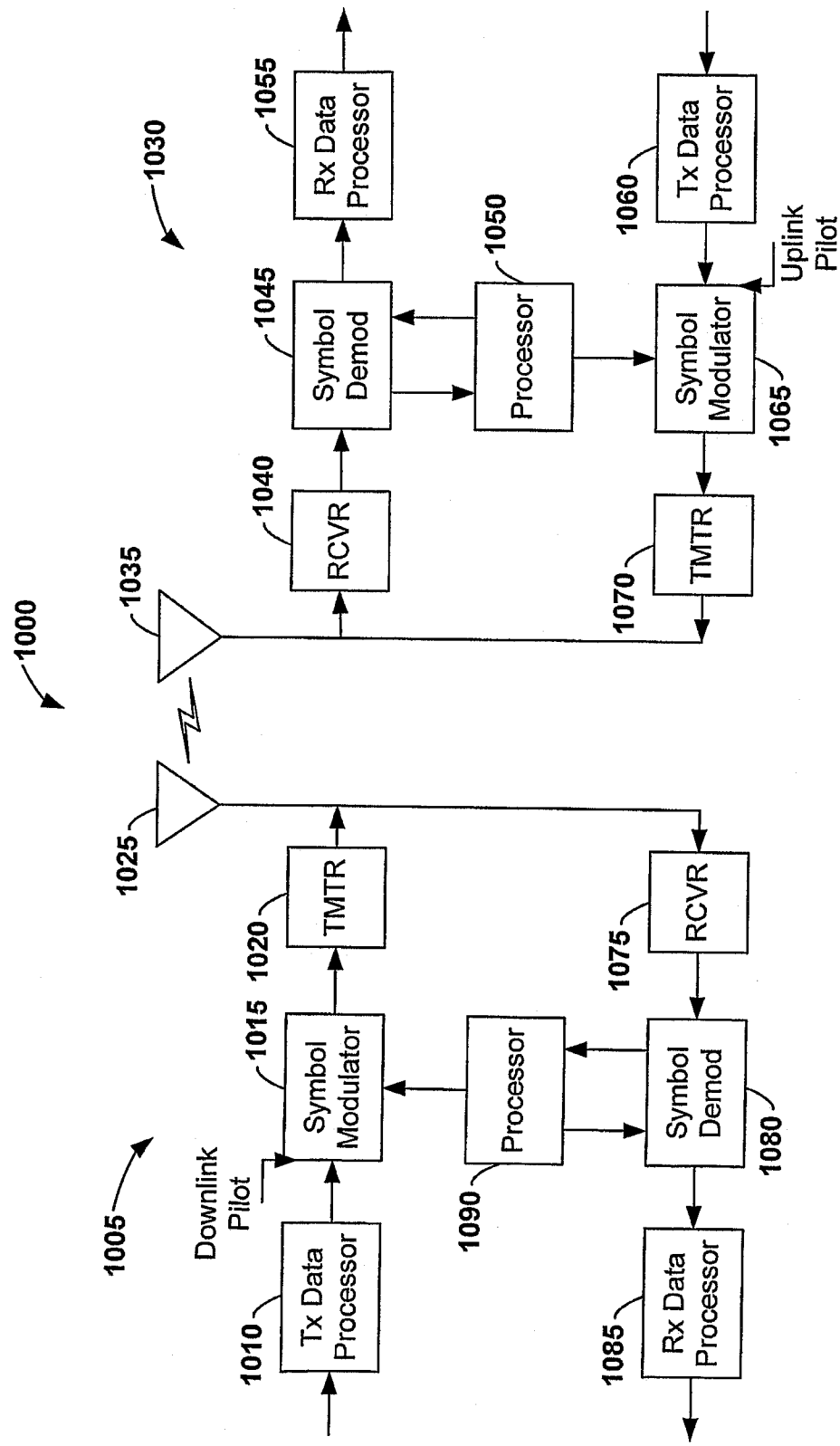

1000
1005
1010
Tx Data Processor
Downlink Pilot
1015
Symbol Modulator
1020
TMTR
1025
1030
1035
1040
RCVR
1045
Symbol Demod
1050
Processor
1055
Rx Data Processor
1060
Tx Data Processor
Uplink Pilot
1065
Symbol Modulator
1070
TMTR
1075
RCVR
1080
Symbol Demod
1085
Rx Data Processor
1090
Processor

FIG. 10