PHASE DETECTOR ARCHITECTURE FOR PHASE ERROR ESTIMATING AND ZERO PHASE RESTARTING

ABSTRACT

A system and method for enabling an efficient Zero Phase Restart (ZPR) of a device. The structure is based on deploying normalized timing gradient (NTG) blocks (501 and 502) in pairs, each circuit employing an orthogonal phase error transfer function characteristic (having one TG circuit sample orthogonally in relation to the other), for example, PR4 and EPR4 modes ideal sampling instances of a preamble. Through iteration of the method of the invention, a NTG block (501 or 502) is selected based on having a native timing sampling instance with a phase error that is closest to zero. Since there is an equal chance that either of the circuits in a circuit pair will be selected, if the circuit implementing the current non-native architecture is selected, a separate signal is generated. This signal adds the equivalent of 180° to the error value that is provided to the timing recovery circuit. For example, by iterating the process after the special case of a zero phase restart (ZPR) operation, the native sampling instance is "forced" to be selected thereafter.

FIGURE 5