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(54) STEREO DEMODULATOR CIRCUIT

(71) We, MOTOROLA, INC., a corporation of the States of Delaware, United States of America, of 5725 North East River Road, Chicago, Illinois 60631, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a stereo demodulator circuit for use in a stereo and monaural sound reproduction system. Stereophonic signals such as stereophonic music programmes from a transmitter provide entertainment. These signals are designed to facilitate compatible monaural and stereophonic reception in FM receivers. The composite stereo signal is defined as including a main channel summation signal, a continuous wave pilot signal, and a subchannel double sideband signal. More specifically, a left audio source and a right audio source, e.g., a disc recording or magnetic tape, which may be located at a transmitter, respectively provide a left (L) and a right (R) channel stereo signal. These two signals are applied to a linear matrix which provides a main channel signal which is equal to the sum of the left and right signals (L + R) and a subchannel signal which is equal to the difference between the left and right signals (L — R). In this system, the (L + R) signals have frequencies ranging between approximately 50 Hz and 15 kilohertz (kHz). The subchannel signal is applied along with a 38 kilohertz subcarrier to a balanced modular, which produces a double sideband, suppressed carrier output signal comprising the subchannel sideband signal. The main channel signal, the subchannel sideband signal and a 19 kHz pilot carrier are then added together and transmitted as an FM modulation on a station carrier whose frequency is between 88 and 108 megahertz. Monaural type receivers then select and demodulate the main channel signal to provide monaural reception. Alternatively, stereophonic receivers select and demodulate a combination of the main channel and subchannel sideband signals to provide left and right stereo output signals. To provide this function, it is necessary to multiply the subchannel sidebands with a 38 kilohertz signal which is phase related to the 19 kilohertz pilot signal. The foregoing multiplication is generally performed only if the received signal is indeed a stereo encoded signal and if it is of sufficient amplitude. This is because the multiplying process can translate some of the high frequency noise occurring in the FM detected spectrum into the audio frequency band thereby degrading the signal-to-noise ratio of the receiver.

Thus, modern stereophonic receivers are equipped with "stereo-mute" circuitry, which deteots the presence of an adequate stereo signal and which suppresses the multiplication process in the absence of an adequate level of such a signal. Unfortunately, because of the configuration of some present day stereo demodulator circuits, a transient signal is produced whenever the multiplication process is initiated and terminated. These transients result in audible clicks which often have magnitudes comparable with the magnitude of the left and right stereo signals and hence can cause undesirable sounds to occur at the loudspeakers of the stereophonic system.

A further problem is created by some prior art demodulators. More specifically, while the multiplication process is inhibited, the received signal tends to pass through transistors of prior art demodulator circuits. This is because even though the demodulator circuit is disabled, the transistors thereof are often biased in an intermediate state between saturation and nonconduction. Consequently, a significant unbalance can result between the output signals of the seereeo

demodulator circuit and these signals can also be distorted. In discrete circuits, it is possible to solve the foregoing problems by carefully choosing components such as transistors and biasing resistors so that perfect balance is obtained in the demodulator circuit. This technique is costly and incompatible with the present trend toward providing stereo demodulators either at consumer prices or in integrated circuit form. More particularly, present day integrated circuit processing provide transistors and resistors having parameter values that extend over certain tolerance ranges. Hence, because of the variations in the process of manufacture, devices which are intended to have identical parameters in a particular circuit can have parameters which in reality are somewhat different.

A need exists to develop a solution to the problems caused by transient signals, imbalances and distortions generated by prior art demodulator circuits due to the component tolerances of said circuits. Moreover, some prior art demodulator configurations are not flexible enough to be operated by a variety of stereo decoding signals.

According to the present invention there is provided a stereo demodulator circuit for use in a stereo and monaural sound reproduction system comprising signal supply means for supplying composite stereo or monaural signals, said composite stereo signals including main channel information signals and sub-channel suppressed carrier information signals, a multiplier circuit having input terminals adapted to receive said composite stereo signals from said signal supply means and a stereo decoding signal, said multiplier circuit including means for multiplying said composite stereo signals and said stereo decoding signal to provide differential sub-channel information signals at outputs thereof, a differential amplifier circuit having first and second input and output terminals respectively which is responsive to the differential sub-channel information signals being applied to said first and second input terminals for providing antiphased sub-channel information signals at said output terminals respectively, matrix summing means coupled to said output terminals of said differential amplifier circuit and arranged to receive either said composite stereo signals or monaural signals from said signal source for summing said composite stereo signals with said antiphased sub-channel information signals from said differential amplifier circuit to provide left and right channel stereo signals, respectively, at the outputs of said matrix summing circuit, and means to hold the multiplier circuit means in either an open or a short circuit state to inhibit multiplication of the composite stereo signals and said stereo decoding signal such that no differential sub-channel information signals are produced at the output terminals of the differential amplifier circuit during the inhibited state of the multiplier circuit and such that output signals are produced from the demodulator circuit only via the matrix summing circuit and not via the differential amplifier circuit.

demodulator circuitry of the invention render it suitable for utilising either a binary or two-level stereo decoding signal, two antiphase binary stereo decoding signals or a tri-level stereo decoding signal. All of the configurations of the demodulator circuit of the invention have the advantage that the output signal quality is not deleteriously affected by the multiplier being enabled and disabled.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

Figure 1 is a block diagram of a stereophonic receiver including a prior art stereo demodulating circuit shown in schematic form;

Figure 2 is a partial block and partial schematic diagram illustrating a stereo demodulator circuit of one embodiment of the invention;

Figure 3 is a partial block and partial schematic diagram illustrating the stereo demodulator circuit of another embodiment of the invention and

Figure 4 is a partial block and partial schematic diagram illustrating a stereo demodulator circuit of still another embodiment of the invention.

A stereophonic receiver will first be described. Then a prior art demodulator circuit will be described along with some of the problems therewith so that the advantages some of the problems therewith so that the advantages of the demodulator circuit structures of the present invention can be more fully appreciated. Referring to Fig. 1, there is shown a stereophonic multiplex receiver including a prior art demodulator circuit in the form of an integrated circuit which is enclosed by dotted lines. A frequency modulated (FM) carrier wave contains a main channel or sum signal of the left and right audio signals (L + R), a subchannel or difference signal of the left and right audio signals (L − R), which is amplitude modulated on a supressed subcarrier wave, and a pilot signal having a frequency one half that of the suppressed subcarrier frequency. This wave is received by antenna 10 and is applied to receiver "front end" circuit 11 which includes an RF amplifier, converter, IF amplifier and limiter which may all be of designs well known in the art. The output of circuit 11 is then supplied to an FM detector and preamplifier circuit 12

where the composite stereo signal is detected.

When stereophonic signals are detected by detector 12, the 19 kc. pilot component is then separated by 19 kc. signal separating circuit 13, which may include a filter circuit tuned to the 19 kc. signal frequency. The output of the 19 kc. signal separator is supplied to frequency doubler 14 which reconstructs the suppressed subcarrier 38 kc. signal, which may be used as the "stereo decoding signal". The frequency doubler 14 should be of a type which provides a symmetrical output signal in order to provide the best possible SCA, or "storecast", rejection in the system with which it is used.

The composite stereo signal is supplied from the output terminal of detector and preamplifier stage 12 over a lead 16, through coupling resistor 17 to the base of an input NPN transistor 18 and to audio mute circuit 23 which shorts the base of transistor 18 to a.c. ground in response to the magnitude of the FM signal decreasing below a predetermined threshold. A stable direct current collector potential for transistor 18 is obtained from voltage reference string 20.

Transistor 18 is operated as an emitter follower and the composite stereo signals present across its emitter resistor 19 are applied to the base of a first demodulator input transistor 22. The collector of the transistor 22 is connected to the emitters of a pair of transistors 24 and 26 which are operated as a first gated synchronous demodulator 28. The 38 kc. stereo decoding signal obtained from the output of frequency doubler circuit 14 provides gating signals for demodulator 28. The base of the transistor 25 is supplied with a constant d.c. reference potential through lead 30.

The operation of the demodulator circuit 28 in such that the 38 kc. gating signal applied thereto from frequency doubler circuit 14 is effective on each cycle to alternately render transistors 24 and 26 conductive and nonconductive. Transistor 26 is cut off, due to the differential action of the transistors 24 and 26, when transistor 24 is driven to conduction and vice versa. At the same time, transistor 22 is operated Class A so that the composite stereo signals present at the collector of the transistor 22 are coupled through the fully turned on transistor 24 or 26 to corresponding output terminals 32 or 34. Right and left audio frequency amplifiers 36 and 38 are connected to output terminals 32 and 34 and amplify the demodulated stereo signals developed across load resistors 41 and 42 which are connected to output terminals 32 and 34. The output terminals of amplifiers 36 and 38 are coupled to loudspeakers 40 and 44. Thus, the 38 kc. stereo decoding signal from frequency doubler 14, gates demodulator transistors 24 and 26 to separate the R signal components from the L signal components.

Synchronous demodulator 28 produces a substantially equal and predictable amount of undesirable crosstalk at each of the output terminals 32 and 34. To eliminate or substantially reduce the crosstalk present in the output signals of demodulator 28, a second synchronous demodulator 46 is provided and includes a second pair of switching transistors 48 and 50 which correspond to transistors 24 and 26 in demodulator circuit 28. The emitters of the transistors 48 and 50 are supplied with signals from the collector of a second demodulator input transistor 52, the base of which is connected to a source of direct current reference potential obtained from the bias string 20. Input signals for driving second demodulator input transistor 52 are coupled to the emitter thereof through a resistive T network consisting of resistors 54, 56 and 58. This resistor network applies the composite stereo signal in atenuated form to the emitter of the transistor 52. The values of resistors 54, 56 and 58 are chosen to provide a predetermined amount of attenuation which causes the L and R signal appearing at the collectors of transistors 48 and 50 to be equal in magnitude and opposite in polarity to the crosstalk signal components appearing at the collectors of transistors 24 and 26. As a consequence, the crosstalk is attenuated. If transistors 24, 26, 48 and 50 could be closely matched, the composite stereo signal or monaural signal appearing at nodes 32 and 34 would have equal amplitudes. Audio frequency amplifiers 36 and 38 would then produce equal drive signals of equal amplitudes for speakers 40 and 44, respectively.

Due to process variations, transistor pairs 24 and 26 and 48 and 50 do not have identical parameters. In monaural operation, when no switching or stereo decoding signals are applied from frequency doubler 14 to demodulator 21, uneven current sharing results between transistor pairs 24 and 26 and 48 and 50. This causes an undesirable unbalance of both the a.c. and d.c. components of the output currents at output terminals 32 and 34. In addition, the amount of unbalance of current sharing between transistor pairs 48 and 50 and 24 and 26 is a function of the level of the magnitude currents conducted by transistors 22 and 52. This non-linearity produces distortion in the demodulator output currents. Thus, the monaural signals supplied to the left audio amplifier 38 and to the right audio amplifier 36 are of unequal amplitudes and are distorted. Thus, although demodulator 21 operates satisfactorily in many applications, this unbalance and distortion under monaural operation somewhat decreases the attractiveness of circuit 21 for use in high

fidelity stereo receivers.

As the stereo decoding signal is inhibited by stereo mute circuit 15, a bias potential is applied to the bases of transistors 24 and 48 by frequency doubler 14. The bias from doubler 14 has a magnitude equal to the bias from circuit 20. Because of the unbalanced condition within the demodulator, a transient is created by the resulting difference in d.c. potentials at nodes 32 and 34 as the demodulator changes from the balanced stereo condition to the unbalanced monaural condition. Similar transients occur when multiplication is re-initiated. These transients have significant magnitudes as compared to the magnitudes of the recovered audio signals. Thus, these transient responses can create undesired noise or audible clicks in speakers 40 and 44 as the demodulator changes back and forth between its monaural and stereo modes of operation.

Figure 2 illustrates a stereo demodulator of one embodiment of the invention which eliminates or reduces the preceding problems and which could replace demodulator 21 in the receiver of Fig. 1. The composite stereo or monaural signals are applied by FM detector 12 or some other signal supply, shown schematically by generator 74 through coupling resistors 76 and 78 to terminals 86 and 88. These signals are also applied to resistors 92 and 94 by conductors 91 and 93. The two multiplier or chopper transistors 80 and 82 are connected between bias terminal 84 and terminals 86 and 88, respectively. Transistors 80 and 82 may be operated in the inverted mode in order to obtain low offset collector-to-emitter voltages during conductive operation. Inverted mode simply means that the collector and emitter electrodes of the transistors are interchanged to cause the emitter electrode to perform the collector function and vice versa. Bias terminal 84 is adapted to receive a constant d.c. potential from a supply of known configuration.

Transistors 80 and 82 are switched between on and off conditions by two antiphase 38 kHz stereo decoding signals applied to the bases thereof by frequency doubler 14, for instance. Because of the phase relationship between the 38 kHz stereo decoding signals, one of chopper transistors 80 or 82 is in an on state while the other chopper transistor is in an off state. If chopper transistor 80 is in the on condition, terminal 86 is connected to bias terminal 84. Since terminal 84 provides an a.c. ground, the composite stereo signal does not appear at terminal 86. Simultaneously, the composite stereo signal does appear at terminal 88 because multiplying transistor 82 is in an off condition. During the next half cycle of the stereo decoding signals, transistor 80 is rendered nonconductive and transistor 82 is conductive. By multiplying the composite signal and the 38 kHz signal, a differential signal comprising the subchannel (L − R) information is developed between terminals 86 and 88. The differential subchannel (L − R) signals are applied to the bases of transistors 108 and 110 of differential amplifier 90. This subchannel information is then amplified by differential amplifier 90 providing in phase and antiphase subchannel (L − R) information components at nodes 95 and 97 which are connected to collector resistors 92 and 94. The left minus right signal (L − R) or subchannel signal and the negative of the left minus right signals — (L − R) or inverted subchannel signals are matrixed with the main channel signal conducted by resistors 92 and 94 at nodes 95 and 97. This results in a left (L) channel signal at node 97 and a right (R) channel signal at node 95 which are supplied to current amplifiers 96 and 98. Current amplifiers 96 and 98 could be replaced by voltage amplifiers provided the appropriate voltage level shifts and gains are affected in order to prevent saturation of transistors 108 and 110 of differential amplifier 90.

To inhibit multiplication in response to weak stereophonic conditions or monaural conditions, transistors 80 and 82 are each held in either an open or short circuit state by, for instance, frequency doubler 14. The short circuit state is preferred because it causes the voltages at the emitters of transisters 80 and 82 to be defined with greater precision. These emitter voltages are the input voltages of the summing circuit. In the inhibited or disabled mode, no subchannel differential signals are impressed between the bases of differential transistors 108 and 110. Therefore, no subchannel information appears at the outputs of differential amplifier 90. The composite stereo signal or monaural signal supplied by generator 74 is applied through resistors 92 and 94 to the input terminals of current amplifiers 98 and 96.

One significant improvement provided by the embodiment of Fig. 2 over the prior art is the reduction of the imbalance between monaural signal levels developed at output terminals 112 and 114, which therefore minimizes the imbalance in the sound levels at speakers 40 and 44. The monaural balance in the circuit of Fig. 2 is a function of the value of resistors 92 and 94, which can be matched to a high degree during the process of manufacture. Also since resistors 92 and 94 have linear transfer characteristics, they contribute virtually no distortion to a monaural signal even if mismatched a small amount.

As an aside, if current amplifiers 96 and 98 are replaced by voltage amplifiers, the monaural signal from supply 74 will appear

at nodes 95 and 97 with virtually no attenuation. Consequently, the monaural signal would be more nearly balanced and be less distorted. However, the use of voltage amplifiers requires level shifting of the composite stereo signal to prevent saturation of transistors 108 and 110.

If a symmetrical stereo decoding signal is applied to transistors 80 and 82 of the circuit of Fig. 2, the transient responses that occur in prior art circuits during the process of switching between stereo and monaural reception are significantly reduced and become inaudible. More specifically, the d.c. components at the collector of transistors 108 and 110 are nearly unaffected by the initiation and inhibition of the multiplier action. This is because any differential d.c. voltage change appearing between terminals 86 and 88 during switching between stereo and monaural operation as a result of process variations or imbalances between resistors 76 and 78 is severely degenerated by the negative feedback provided by emitter resistors 100 and 102.

Another significant advantage of the embodiment of Fig. 2 is that the stereo decoding signals used therewith can be of different phase or form provided that their d.c. components are equal. Thus, this demodulator circuit can be driven by 38 kHz fifty percent duty cycle square wave stereo decoding signals displaced by 60 degrees which thereby provide cancellation of the third harmonic of the stereo decoding signal, as described in U.K. patent application No. 11217/75 (Serial No. 1494570).

In Figs. 3 and 4, the same reference numbers are used for components corresponding to like components of Fig. 2. The structure of the circuit of Fig. 3 is the same as Fig. 2 except that transistor 83 has a conductivity which is opposite to the conductivity of transistor 80 and the bases of transistors 80 and 83 are connected together. These differences enable the use of a three-level stereo decoding signal which can have low, reference and high levels. More particularly, if the stereo decoding signal is "high", transistor 80 is rendered conductive and transistor 83 is nonconductive. If the stereo decoding signal is at a reference level, which is approximately equal in magnitude to the bias potential, neither transistor 80 nor 83 is conductive. If the stereo decoding signal is "low", transistor 83 is conductive and transistor 80 is nonconductive. The circuit of Fig. 3 can operate as a three-level multiplier because it requires only one trilevel drive signal whereas the circuit of Fig. 2 would require two separate tri-level drive signals to eliminate the undesired 114 kHz response Otherwise the circuit of Figure 3 functions identically to that of Figure 2.

The configuration of the circuit of Fig. 4 differs from the configuration of the circuit of Fig. 2 in that resistor 104 is exchanged for current source 91 and the output terminal of composite stereo supply 74 is not directly connected to collector resistors 92 and 94. Also, collector resistors 92 and 94 are connected to bias conductor 111.

In the previous embodiments of Figs. 2 and 3, the matrix summing of the main and subchannel signals is accomplished in the output circuits of differential amplifier 90. However, in the embodiment of Fig. 4, the matrix summing occurs in the emitter circuit of differential amplifier 90. More specifically, during stereo operation, the composite stereo signals from generator 74 are multiplied by the stereo decoding signals gated through transistors 80 and 82 to derive the differential subchannel (L − R) signals that are impressed onto the bases of transistors 108 and 110 of amplifier 90. The subchannel (L − R) information is then amplified by differential amplifier 90 to provide in phase and antiphase subchannel (L − R) information components at the colectors of transistors 108 and 110. The main channel (L + R) information of the composite stereo signal, which is applied as a common mode input, appears in phase on the bases of transistors 108 and 110 and across resistor 104 to produce a common mode current signal at node 106. This common mode current is divided equally between transistors 108 and 110 and creates in phase main channel collector outputs. The common mode (L + R) signals are added at node 106 to the subchannel signals, (L − R), and to the inverted subchannel signals — (L − R), to cause the left channel and right channel stereo output signals at output terminals 112 and 114 of differential amplifier 90.

During monaural operation, chopper transistors 80 and 82 must be held in an off condition by the driving circuit thereby enabling the main channel (L + R) information to be applied to the input terminals of differential amplifier 90. The amplified monaural information occurs at output terminals 112 and 114.

Direct current differential voltage changes that appear between terminals 86 and 88 during switching from stereo operation to monaural operation as a result of process variations or imbalance between resistors 76 and 78 are severely degenerated by the negative feedback provided by resistors 100 and 102.

The circuits of Fig. 2, Fig. 3, and Fig. 4 all utilize the same method of demodulation. More specifically, a stereo decoding signal is first derived, for instance, by blocks 13 and 14 of Fig. 1 or by the systems described in the aforementioned related patent application. The composite stereo signal is multi-

plied by the stereo decoding signal in the multiplier by transistor 80 and either transistor 82 or 83 to form a subchannel signal at the bases of transistors 108 and 110 of differential amplifier 90. Transistor 108 amplifies the non-inverted subchannel signal which is then added to the composite stereo signal to form a left channel output stereo signal. Transistor 110 provides an inverted subchannel signal which is added to the composite stereo signal to form a right channel stereo signal.

What has been described, therefore, are improved stereo demodulator circuits which are suitable for manufacture in integrated circuit form. The demodulator circuit configurations of Figs. 2 and 3 do not provide an undesirable amount of distortion to a monaural signal being passed therethrough because this signal is conducted through a resistive network rather than through active transistors. Moreover, negative feedback is employed in all of the demodulator configurations to reduce distortion. In addition, the resistive networks and negative feedback tend to prevent undesirable transients from being created as the stereo decoding signal is applied and removed from the demodulator circuit. Also, the stereo demodulator circuit configurations provide improved match between monaural signal levels occurring at the output terminals of the demodulator and are flexible enough to be operated by single phase, multiphase and three-level stereo demodulating signals. All of the disclosed circuit configurations utilise the same method of demodulation which is described above.

WHAT WE CLAIM IS:—

1. A demodulator circuit for use in a stereo and monaural sound reproduction system comprising signal supply means for supplying composite stereo or monaural signals, said composite stereo signals including main channel information signals and subchannel suppressed carrier information signals, a multiplier circuit having input terminals adapted to receive said composite stereo signals from said signal supply means and a stereo decoding signal, said multiplier circuit including means for multiplying said composite stereo signals and said stereo decoding signal to provide differential subchannel information signals at outputs thereof, a differential amplifier circuit having first and second input and output terminals respectively which is responsive to the differential sub-channel information signals being applied to said first and second input terminals for providing antiphased sub-channel information signals at said output terminals respectively, matrix summing means coupled to said output terminals of said differential amplifier circuit and arranged to receive either said composite stereo signals or monaural signals from said signal source for summing said composite stereo signals with said antiphased sub-channel information signals from said differential amplifier circuit to provide left and right channel stereo signals, respectively, at the outputs of said matrix summing circuit, and means to hold the multiplier circuit means in either an open or a short circuit state to inhibit multiplication of the composite stereo signals and said stereo decoding signal such that no differential sub-channel information signals are produced at the output terminals of the differential amplifier circuit during the inhibited state of the multiplier circuit, and such that output signals are produced from the demodulator circuit only via the matrix summing circuit and not via the differential amplifier circuit.

2. A demodulator circuit as claimed in claim 1 wherein said multiplier circuit includes: first transistor control means having first, second and control electrodes; second transistor control means having first, second and control electrodes, said first electrodes of said first and second transistor control means being coupled to said input terminals of said differential amplifier circuit, said second electrodes of said first and second transistor control means being interconnected and said respective control electrodes being adapted to receive said stereo decoding signal, said composite stereo signals being applied between said interconnected electrodes and said first electrodes of said first and second transistor control means and said first and second transistor control means and said first and second electron control means being alternately rendered conductive and non-conductive by said stereo decoding signal.

3. A demodulator circuit as claimed in claim 2 wherein said stereo decoding signal comprises a third harmonic free signal, said signal being at substantially the frequency of said suppressed carrier frequency and said first and second transistor control means of said multiplier being rendered in a non-operative state when said multiplier circuit is inhibited to prevent said differential subchannel signals being applied to said differential amplifier.

4. A demodulator circuit as claimed in claim 2 wherein said control electrodes of said first and second transistor control means of said multiplier circuit are interconnected and adapted to receive said stereo decoding signal, said stereo decoding signal having low, reference and high levels, respectively.

5. A monolithic demodulator circuit suitable to be utilized in a sound reproduction system, comprising: a multiplier circuit which includes first and second transistors, the collector electrodes of said first and second transistors being interconnected, said multiplier circuit being adapted to receive

plied by the stereo decoding signal in the multiplier by transistor 80 and either transistor 82 or 83 to form a subchannel signal at the bases of transistors 108 and 110 of differential amplifier 90. Transistor 108 amplifies the non-inverted subchannel signal which is then added to the composite stereo signal to form a left channel output stereo signal. Transistor 110 provides an inverted subchannel signal which is added to the composite stereo signal to form a right channel stereo signal.

What has been described, therefore, are improved stereo demodulator circuits which are suitable for manufacture in integrated circuit form. The demodulator circuit configurations of Figs. 2 and 3 do not provide an undesirable amount of distortion to a monaural signal being passed therethrough because this signal is conducted through a resistive network rather than through active transistors. Moreover, negative feedback is employed in all of the demodulator configurations to reduce distortion. In addition, the resistive networks and negative feedback tend to prevent undesirable transients from being created as the stereo decoding signal is applied and removed from the demodulator circuit. Also, the stereo demodulator circuit configurations provide improved match between monaural signal levels occurring at the output terminals of the demodulator and are flexible enough to be operated by single phase, multiphase and three-level stereo demodulating signals. All of the disclosed circuit configurations utilise the same method of demodulation which is described above.

WHAT WE CLAIM IS:—

1. A demodulator circuit for use in a stereo and monaural sound reproduction system comprising signal supply means for supplying composite stereo or monaural signals, said composite stereo signals including main channel information signals and subchannel suppressed carrier information signals, a multiplier circuit having input terminals adapted to receive said composite stereo signals from said signal supply means and a stereo decoding signal, said multiplier circuit including means for multiplying said composite stereo signals and said stereo decoding signal to provide differential subchannel information signals at outputs thereof, a differential amplifier circuit having first and second input and output terminals respectively which is responsive to the differential sub-channel information signals being applied to said first and second input terminals for providing antiphased sub-channel information signals at said output terminals respectively, matrix summing means coupled to said output terminals of said differential amplifier circuit and arranged to receive either said composite stereo signals or monaural signals from said signal source for summing said composite stereo signals with said antiphased sub-channel information signals from said differential amplifier circuit to provide left and right channel stereo signals, respectively, at the outputs of said matrix summing circuit, and means to hold the multiplier circuit means in either an open or a short circuit state to inhibit multiplication of the composite stereo signals and said stereo decoding signal such that no differential sub-channel information signals are produced at the output terminals of the differential amplifier circuit during the inhibited state of the multiplier circuit, and such that output signals are produced from the demodulator circuit only via the matrix summing circuit and not via the differential amplifier circuit.

2. A demodulator circuit as claimed in claim 1 wherein said multiplier circuit includes: first transistor control means having first, second and control electrodes; second transistor control means having first, second and control electrodes, said first electrodes of said first and second transistor control means being coupled to said input terminals of said differential amplifier circuit, said second electrodes of said first and second transistor control means being interconnected and said respective control electrodes being adapted to receive said stereo decoding signal, said composite stereo signals being applied between said interconnected electrodes and said first electrodes of said first and second transistor control means and said first and second transistor control means and said first and second electron control means being alternately rendered conductive and non-conductive by said stereo decoding signal.

3. A demodulator circuit as claimed in claim 2 wherein said stereo decoding signal comprises a third harmonic free signal, said signal being at substantially the frequency of said suppressed carrier frequency and said first and second transistor control means of said multiplier being rendered in a non-operative state when said multiplier circuit is inhibited to prevent said differential sub-channel signals being applied to said differential amplifier.

4. A demodulator circuit as claimed in claim 2 wherein said control electrodes of said first and second transistor control means of said multiplier circuit are interconnected and adapted to receive said stereo decoding signal, said stereo decoding signal having low, reference and high levels, respectively.

5. A monolithic demodulator circuit suitable to be utilized in a sound reproduction system, comprising: a multiplier circuit which includes first and second transistors, the collector electrodes of said first and second transistors being interconnected, said multiplier circuit being adapted to receive

applied composite signals which include main channel signal information and subchannel suppressed carrier signal information which is coupled between said interconnected collector electrodes and the respective emitter electrodes of said first and second transistors, said multiplier circuit being adapted to receive an applied driving signal between the base electrodes of said transistors for alternately switching said first and second transistors between conductive and nonconductive states when said composite signal is received and for causing said first and second transistors to both be in a predetermined nonoperative state in the absence of said composite signals, said multiplier circuit providing differential subchannel information signals between said emitter electrodes of said first and second transistors; a differential amplifier circuit having inputs connected to the emitters of said first and second transistors of said multiplier circuit for providing antiphased subchannel information signals at first and second outputs respectively; and a summing matrix coupled to said first and second outputs of said differential amplifier for summing said composite signal with said antiphased subchannel information signals to derive right and left channel stereophonic audio signals respectively at said first and second outputs of said differential amplifier.

6. A demodulator circuit as claimed in claim 5 wherein said summing matrix includes first and second resistors, said first and second resistors being directly coupled at one terminal thereof to said first and second outputs respectively of said differential amplifier, said first and second resistors having the other terminals thereof adapted to receive said applied composite signals or monaural signals.

7. A demodulator circuit as claimed in claim 5 or 6 wherein said first and second transistors of said multiplier circuit are NPN transistors.

8. A demodulator circuit as claimed in claim 5 or 6 wherein said first transistor is a NPN transistor, said second transistor is a PNP transistor and said driving signal being at essentially the same frequency of said suppressed carrier and having first, intermediary and second magnitude levels associated therewith.

9. A demodulator circuit for providing left and right channel stereo signals comprising a multiplier circuit for multiplying a composite stereo signal and a stereo decoding signal applied thereto to provide differential sub-channel information signals at first and second outputs, a differential amplifier circuit for providing said left and right channel stereo signals at first and second outputs thereof, said differential amplifier circuit including a first electron control device having first, second and control electrodes, a second electron control device having first, second and control electrodes, said control electrodes of said first and second electron control devices being coupled respectively, to said first and second outputs of said multiplier circuit, said second electrode of said first and second electron control devices being coupled respectively to said first and second outputs of said differential amplifier circuit, a resistive tee network coupled to said first electrodes of said differential amplifier circuit, said differential sub-channel information signals being summed with a common moded composite stereo signal appearing across said resistive tee network such that the left and right channel stereo signals are provided.

10. A demodulator circuit as claimed in claim 9 wherein said multiplier circuit includes first and second electron control devices each having first, second and control electrodes, said second electrodes of said first and second electron control devices being coupled to each other, said composite stereo signal being applied between said second electrodes of said first and second electron control devices and respective first electrodes of said first and second electron control devices, said stereo decoding signal being applied to said control electrodes of said first and second electron control devices for alternately rendering said devices conductive and non-conductive to provide said multiplication said first and second control devices being held in an off state to inhibit multiplication.

11. A demodulator circuit substantially as hereinbefore described and as shown in any of Figures 2 to 4 of the accompanying drawings.

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