# CIRCUIT STRUCTURE AND FABRICATION METHOD THEREOF

## INCORPORATION BY REFERENCE

**[0001]** The publications noted in the disclosure herein are each fully incorporated by reference, as if fully set forth in its entirety herein.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

**[0002]** The present invention relates to semiconductor devices, particularly to structures of semiconductor devices, and more particularly to post passivation structures for semiconductor devices and packaging processes for such.

### 2. Description of Related Art

**[0003]** Semiconductor wafers are processed to produce IC (integrated circuit) chip having ever-increasing device density and shrinking feature geometries. Multiple conductive and insulating layers are required to enable the interconnection and isolation of the large number of semiconductor devices in different layers (e.g., active and passive devices, such as TFT, CMOS, capacitors, inductors, resistors, etc). Such large scale integration results in increasing number of electrical connections between various layers and semiconductor devices. It also leads to an increasing number of leads to the resultant IC chip. These leads are exposed through a passivation layer of the IC chip, terminating in I/O pads that allow connections to external contact structures in a chip package.

**[0004]** Wafer-Level Packaging (WLP) refers to the technology of packaging an IC chip at wafer level, instead of the traditional process of assembling the package of each individual unit after wafer dicing. WLP allows for the integration of wafer fabrication, packaging, test, and burn-in at the wafer level, before being singulated by dicing for final assembly into a chip carrier package (e.g., a ball grid array (BGA) package). The advantages offered by WLP include smaller size (reduced footprint and thickness), lesser weight, relatively easier assembly process, lower overall production costs, and improvement in electrical performance. WLP therefore

streamlines the manufacturing process undergone by a device from silicon start to customer shipment. While WLP is a high throughput and low cost approach to IC chip packaging, it however invites significant challenges in manufacturability and structural reliability.

**[0005]** WLP basically consists of extending the wafer fabrication processes to include device interconnection and device passivation processes. The first step to WLP is to enlarge the pad pitch of standard ICs by redistribution technology post passivation of the IC semiconductor structure. Low cost stencil printing of solder or placing preformed solder balls is then possible. Examples of redistribution technology are disclosed, for example, in U.S. Patent No. 6,642,136; U.S. Patent No. 6,784,087; and U.S. Patent No. 6,818,545, commonly assigned to the assignee of the present invention. As disclosed in these patents, a redistribution layer (RDL) contacts the I/O pad of the semiconductor structure. The RDL is supported on a layer of polymer or elastomer deposited over a passivation layer. A contact post is formed on the RDL, using a photo-masking process. The resultant contact post is freestanding, unsupported on its lateral sides. The resultant structure can be further assembled into a chip carrier package using flip chip assembly technique. While the post passivation structures and related processes provide for IC packaging with improved pitch resolution, there is still a limitation to meeting the increasing demand for finer pitch resolution in view of the ever increasing scale of integration in ICs. There is also potential risk for stress-induced failures, as noted below.

**[0006]** U.S. Patent No. 6,103,552 discloses another WLP process including a post passivation RDL. The RDL is supported on a layer of polymeric material that is deposited on the passivation layer of the semiconductor structure. Another polymeric layer is deposited over the RDL, and etched or drilled to provide a via for over-filling with a metal to form an interconnect (i.e., a conducting post) that extends above and beyond the opening of the via. The top polymeric layer and the bottom polymeric layer are separated by a layer of chrome-copper, and therefore do not touch between the RDL structures. A solder bump attached to the protruding end of the post is formed by electroless plating, screen or stencil printing. Because the post extends beyond the surface of the polymeric layer, and the top surface of the structure is otherwise not smooth, high-resolution lithography cannot be achieved to form the vias for the conductive posts and to plate the solder bumps. Consequently, the pitch of the contacts for the IC package would be limited. This limitation would be more pronounced with an increase in thickness of the polymeric layer,

which otherwise may be desirable to provide better stress relief, as discussed below. Further, as noted, the bottom polymeric layer is separate from the top polymeric layer, therefore the bottom polymeric layer alone does not provide good stress relief. If the bottom polymeric layer is made thin to reduce lateral RDL displacements, stress relief would be poor, leading to issues further discussed below.

**[0007]** One of the challenges to structural reliability includes providing adequate stress relief in the resultant WLP processed multilayered structure, including the semiconductor IC die and the additional post passivation structure. For example, the thin film bonded on the passivation layer is subject to biaxial stress that is thermally induced. Equation (1) represents a theoretical mathematical modeling of the biaxial thermal stress in the post passivation thin film in relationship to various physical parameters of the bonded structure on a silicon (Si) substrate:

**[0008]** Equation (1):

$$\sigma_{ppt} = \frac{1}{6R} \frac{Y_s x_{Si}^2}{(1-\nu_{Si}) x_{ppt}}$$

**[0009]** where:

$\sigma_{ppt} = \sigma_x = \sigma_y$ ; biaxial stress in the post passivation thin film;

R= radius of curvature of the Si substrate caused by thermal stress;

$Y_s$= Young's modulus of Si substrate;

$\nu_{si}$= Poisson's ratio of Si substrate;

$x_{Si}$= thickness of Si substrate; and

$x_{ppt}$ = thickness of the post-passivation thin film.

**[0010]** Based on the above formula, there are two ways to lowering the biaxial stress $\sigma_{ppt}$ (in addition to increasing $\nu_{si}$): (a) lower $x_{Si}$, which means making the Si substrate thinner; or (b) increase $x_{ppt}$, which means increasing the thickness of the post-passivation thin film structure.

**[0011]** Fig. 1 schematically shows a prior art post passivation structure 10, including an RDL 12 and a stress-relieving polymer (or stress buffer) layer 14, formed over a passivation layer 16 at the top layer of the semiconductor IC chip 18. The polymer layer 14 is made of, for example, an elastomer, epoxy, low-K dielectric material, or other polymer. Elastomer is used mainly for providing sufficient mechanical flexibility for the bonded structure. As can also be deduced from Equation (1) above, when a polymer layer is deposited over an IC chip 18, the stress generated by the chip and the structure bonded thereto can be absorbed or buffered to reduce local damage to the chip; this in turn enhances the reliability of the structure 10, especially the delicate circuits in the IC chip. According to the relationship set forth in Equation (1), the performance of this buffering effect is increased as the thickness of the polymer layer increases.

**[0012]** There is a generic problem associated with using a thick polymer layer. The RDL 12 shown in Fig. 1 is typically made of copper; it is intended to connect IC I/O pads 20 on the IC chip 18 to external circuitry. When deposited with solder bumps and/or provided with copper conductive post atop at pads 22, the RDL 12 can be bonded to the next level packaging structure firmly (e.g., a chip carrier). The RDL 12 escalates from a lower plane (i.e., the plane with the IC I/O pads 20) to a higher one (the top of the polymer) via a sloping ramp 22 defined by the polymer layer 14. The slope in the ramp 22 is desired for metal step coverage on the sidewall of the thick opening in the polymer layer 14. In practice, the slope of the ramp 22 could vary for each opening in the polymer layer 14, depending on the actual process conditions and inherent physical properties and characteristics of the polymer (e.g., wetting angle, which has to do with the surface energy of the materials). For example, in many cases the slope of the ramp 22 in the polymer layer 14 on the IC passivation layer 16 can be as low as about 45°. Consequently, the RDL 12 must necessarily translate by a significant amount of lateral displacement to extend from the IC I/O pad 20 to the top of the thick layer of polymer 14. Consequently, this lateral displacement necessitates the allowance of a significant amount of tolerance in the layout of the RDL 12. As a result of the tolerance allowance necessary to accommodate the varying slopes of ramps for different openings in the polymer layer 14 and the varying lateral displacements of RDLs, the pitch between adjacent contact structures (e.g., defined by solder bumps and/or copper posts) on the RDLs is limited, and the distances between the contact structures and the openings in the passivation layer are increased. This results in a post passivation structure that does not have fine pitch structures for the next level of packing structure. On the other hand, if a thick

layer of polymer is not used, stress buffering would not be sufficient, leading to possible stress induced failure of the delicate circuits in the IC chip. Further, there would be insufficient lateral support to tall conductive posts, resulting in limited pitch of the I/O structures. It is desirable to have tall conductive posts, as they provide sufficient distance to reduce capacitance coupling between the I/O pads 22 and the electrical circuits in the IC chip 18.

**[0013]** The issues noted above collectively placed a limitation on reducing the pitch of the contact structures achievable on the post passivation structures, and thus also a limitation on increasing the scale of integration of ICs.

**[0014]** It is desirable to provide a WLP structure, and a process relating to same, that allows for both improved stress relief and fine pitch contact structures.

## SUMMARY OF THE INVENTION

**[0015]** The present invention overcomes the drawbacks of the prior art, by providing post passivation structures and related processes that accommodate both stress relief and fine pitch contact structures. In accordance with the present invention, a pitch of <250 μm, and a pin count of >400 may be achieved for the IC packaging.

**[0016]** In one aspect, the present invention provides a post passivation rerouting support structure that comprises a relatively thin support layer (e.g., a polymer layer) above the passivation layer to support fine pitch rerouting structures, and in addition a relatively thick support layer (e.g., a polymer layer) for the fine pitch rerouting structures for next level packaging structure.

**[0017]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a substrate; a first metallic post, formed on the substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a second metallic post, formed on the substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4, wherein the distance between the center of the first metallic post to the center of the second metallic post is 10 to 250microns.

**[0018]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a first metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a second metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; an insulation layer, formed on the semiconductor substrate, and covering the first and second metallic posts; a first bump, formed on the first

metallic post or the insulation layer; and a second bump, formed on the second post or the insulation layer, wherein the distance between the center of the first bump and the center of the second bump is 10 to 250microns.

**[0019]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a first metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a second metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a metallic wire, interconnecting the top of the first metallic post and the top of the second metallic post, wherein the material of the metallic wire includes gold.

**[0020]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a first metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a second metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a metallic wire, interconnecting the top of the first metallic post and the top of the second metallic post; and a polymer layer, formed on the metallic circuit.

**[0021]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4, wherein a conductive wire can be connected to the metallic post or the semiconductor substrate with a wire-bonding method.

**[0022]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention

comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a polymer layer, formed on the semiconductor substrate, and covering the metallic post, wherein a bump 10~150microns high can be formed on the metallic post or the insulation layer.

**[0023]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a polymer layer, formed on the semiconductor substrate, and covering the metallic post; and a metallic coil, formed on the polymer layer, and 1 to 15microns thick.

**[0024]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a bump, formed on the metallic post or the semiconductor substrate, wherein the bump may be a 10 to 30microns thick golden layer.

**[0025]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a bump, formed on the metallic post or the semiconductor substrate, wherein the bump may be a titanium-containing metallic layer.

**[0026]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a bump, formed on the metallic post or the semiconductor substrate, wherein the bump may be a chromium-containing metallic layer.

**[0027]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; and a bump, formed on the metallic post or the semiconductor substrate, wherein the bump may be a tantalum-containing metallic layer.

**[0028]** To achieve the abovementioned objectives, the present invention proposes a circuit structure and a fabrication method thereof. The circuit structure of the present invention comprises: a semiconductor substrate; a metallic post, formed on the semiconductor substrate, and 20 to 300microns high with the ratio of the maximum horizontal dimension thereof to the height thereof less than 4; a first polymer layer, formed on the semiconductor layer, and covering the metallic post; a substrate; a bump, formed between the metallic post and the substrate or formed between the first polymer layer and the substrate; and a second polymer layer, formed between the substrate and the semiconductor substrate, and covering the bump.

**[0029]** To enable the objectives, technical contents, characteristics and accomplishments of the present invention to be more easily understood, the embodiments of the present invention are to be described in detail in cooperation with the attached drawings.

## BRIEF DESCIPTION OF THE DRAWINGS

**[0030]** Fig.1 is a sectional view schematically showing a conventional technology.

**[0031]** Fig.2 is a sectional view schematically showing a semiconductor substrate according to the present invention.

**[0032]** Fig.3 is a sectional view schematically showing that a minute connection structure and a passivation layer are formed the semiconductor substrate according to the present invention.

**[0033]** Fig.4a and Fig.4b are sectional views schematically showing the fabrication procedures of a first polymer layer according to the present invention.

**[0034]** Fig.5 is a sectional view schematically showing the fabrication procedures of a first adhesion/barrier/seed layer according to the present invention.

**[0035]** Fig.6a to Fig.6e are sectional views schematically showing the fabrication procedures of a first RDL and metallic posts according to the present invention.

**[0036]** Fig.7a and Fig.7b are respectively a sectional view schematically showing the parameters of the metallic posts and a top view schematically showing the metallic posts according to the present invention.

**[0037]** Fig.8a is a sectional view schematically showing the fabrication procedures of a second polymer layer according to the present invention.

**[0038]** Fig.8b is a sectional view schematically showing the fabrication procedures of the openings of the second polymer layer according to the present invention.

**[0039]** Fig.8c is a sectional view schematically showing the procedure of polishing the second polymer layer according to the present invention.

**[0040]** Fig.9 is a sectional view schematically showing the fabrication procedures of a third polymer layer according to the present invention.

**[0041]** Fig.10a to Fig.10d are sectional views schematically showing the fabrication procedures of a third metallic layer according to the present invention.

**[0042]** Fig.11 is a sectional view schematically showing that the semiconductor substrate is diced according to the present invention.

**[0043]** Fig.12a to Fig.12c are sectional views schematically showing the fabrication procedures of solder balls according to the present invention.

**[0044]** Fig.12d and Fig.12e are sectional views respectively schematically showing that the semiconductor substrate is diced and that the semiconductor unit is joined to a substrate according to the present invention.

**[0045]** Fig.13a and Fig.13b are sectional views schematically showing the wire-bonding procedures of the metallic posts according to the present invention.

**[0046]** Fig.14a and Fig.14b are sectional views schematically showing the procedures of forming a RDL on the metallic posts according to the present invention.

**[0047]** Fig.13a and Fig.13b are sectional views schematically showing the wire-bonding procedures of the metallic posts according to the present invention.

**[0048]** Fig.15a to Fig.15c are sectional views respectively schematically showing the wire-bonded copper/nickel/gold metallic posts and the wire-bonded copper/gold metallic posts according to the present invention.

**[0049]** Fig.16a to Fig.16h are sectional views schematically showing the fabrication procedures of a first coil-like metallic layer formed above the metallic posts according to the present invention.

**[0050]** Fig.16g is a sectional view schematically showing the fabrication procedures of a second coil-like metallic layer according to the present invention.

**[0051]** Fig.16h is a sectional view schematically showing the procedures of forming a capacitor element on the metallic posts according to the present invention.

**[0052]** Fig.17a to Fig.17d are sectional views schematically showing the fabrication procedures of a metallic layer to interconnect two metallic posts according to the present invention.

**[0053]** Fig.17e to Fig.17m are sectional views schematically showing the procedures of forming a multi-layer circuit on the metallic posts according to the present invention.

**[0054]** Fig.18 is a sectional view schematically showing the procedures of forming a resistor element on the metallic posts according to the present invention.

**[0055]** Fig.19a and Fig.19b are sectional views schematically showing that a portion of the second polymer layer is removed with an etching method according to the present invention.

**[0056]** Fig.19c is a sectional view schematically showing that the semiconductor substrate is diced according to the present invention.

**[0057]** Fig.19d and Fig.19e are sectional views respectively schematically showing the procedures of forming solder balls and dicing the semiconductor substrate according to the present invention.

**[0058]** Fig.19f is a sectional view schematically showing the procedures of forming contact pads according to the present invention.

**[0059]** Fig.19g to Fig.19k are sectional views schematically showing the procedures of forming a metallic layer to interconnect two metallic posts according to the present invention.

**[0060]** Fig.20a is a sectional view schematically showing the procedures of forming a ninth patterned polymer layer on the semiconductor substrate according to the present invention.

**[0061]** Fig.20b to Fig.20d are sectional views schematically showing the procedures of forming the metallic posts with a Damascene method according to the present invention.

**[0062]** Fig.21a to Fig.21d are sectional views respectively schematically showing the structures of the bump, contact pad, solder ball and RDL according to the present invention.

**[0063]** Fig.22 to Fig.25 are sectional views respectively schematically showing the structures of the current freeway, coil, capacitor element, and resistor element according to the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

**[0064]** The present invention pertains to a circuit structure and a fabrication method thereof, wherein multiple metallic posts are formed on a semiconductor substrate, and the spacing between the neighboring metallic posts is reduced to less than 250μm. Below, several embodiments are used to exemplify the present invention.

**Embodiment 1**

**[0065]** Refer to Fig.2. Firstly, a semiconductor substrate 30 is provided, and the semiconductor substrate 30 may be Si substrate, GaAs substrate, GeSi substrate or SOI (silicon-on-insulator) substrate. In Embodiment 1, the semiconductor substrate 30 is a circular semiconductor wafer. The semiconductor substrate 30 has an active surface having multiple electronic elements 32, which are formed via doping trivalent or pentavalent ions, such as boron ions or phosphorus ions. The electronic elements 32 may be MOS transistors, MOS devices, p-channel MOS devices, n-channel MOS devices, BiCMOS devices, Bipolar Junction Transistors, diffusion areas, resistors, capacitors, or CMOS devices.

**[0066]** Refer to Fig.3. A fine-line connection structure 34 is formed on the active surface. The fine-line connection structure 34 comprises multiple thin-film insulating layers 36 having a thickness less than 3μm and multiple thin-film circuit layers 38 also having a thickness less than 3μm. The thin-film circuit layers 38 are made of a copper material or an aluminum material. The thin-film insulating layers 36 are usually formed with a CVD (Chemical Vapor Deposition) method. The material of the thin-film insulating layers 36 may be silicon oxide, TEOS (Tetraethoxysilane), SiwCxOyHz, compound of silicon and nitrogen/compound of silicon, nitrogen and oxygen, SOG (Spin-On Glass), FSG (Fluoro-Silicate Glass), SiLK, black diamond, polyarylene ether, PBO (Polybenzoxazole), or porous silicon oxide. The dielectric constant of the thin-film insulating layers 36 may be lower than 3.

**[0067]** When a damascene process is used to form one of multiple thin-film circuit layers 38 over the semiconductor substrate 30, a diffusion-barrier layer is firstly sputtered on the upper surface of one of the thin-film insulating layers 36 and on the bottoms and the lateral walls of the openings in said one of the thin-film insulating layers 36; next, a seed layer, such as a copper seed layer, is sputtered on the diffusion-barrier layer; next, a copper layer is electroplated on the seed layer; and then, the electroplated copper layer, seed layer and diffusion-barrier layer outside the openings in said one of the thin-film insulating layers 36 are removed with a chemical mechanical polishing method until the upper surface of said one of the thin-film insulating layers 36 is exposed. In another method to form one of multiple thin-film circuit layers 38 over the semiconductor substrate 30, an aluminum layer or an aluminum alloy layer is sputtered on one of the thin-film insulating layers 36; and then, the aluminum layer or the aluminum alloy layer is patterned with a photolithographic process and an etching process. The thin-film circuit layers 38 can be interconnected or connected to the electronic elements 32 via the conductive vias in the thin-film insulating layers 36. The thickness of one of the thin-film circuit layers 38 is generally 0.1~0.5μm. The thin-film circuit layers 38 are fabricated with a 5X stepper or 5X scanner or other superior equipment in the step of a photolithographic process.

**[0068]** Next, a passivation layer 42 is formed over the semiconductor substrate 30 with a CVD method. Multiple contact pads 44 are respectively exposed by openings in the passivation layer 42. The passivation layer 42 can protect the electronic elements 32 on the semiconductor substrate 30 from foreign ion contamination. The passivation layer 42 can retard the penetration of mobile ions (such as sodium ions), moisture, transition metals (such as gold, silver, and copper) and impurities. Thereby, the passivation layer 42 can protect the thin-film circuit layers 38, the thin-film insulating layers 36 and the underlying electronic elements 32 including: transistors, polysilicon resistors, polysilicon-polysilicon capacitors. The passivation layer 42 is usually composed of silicon oxide, compounds of silicon and oxygen, silicate and phosphate glass, silicon nitride, or silicon oxy-nitride, etc. Below, ten methods for depositing the passivation layer 42 are to be introduced.

Method 1

**[0069]** A silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed with a CVD method; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxide with a CVD method.

Method 2

**[0070]** A silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed with a CVD method; next, a silicon oxy-nitride layer with a thickness of between 0.05 and 0.15μm is formed on the silicon oxide with a plasma-enhanced CVD method; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxy-nitride layer with a CVD method.

Method 3

A silicon oxy-nitride layer with a thickness of between 0.05 and 0.15μm is formed with a CVD method; next, a silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxy-nitride layer with a CVD method; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxide layer with a CVD method.

Method 4

**[0071]** A first silicon oxide layer with a thickness of between 0.2 and 0.5μm is formed with a CVD method; next, a second silicon oxide layer with a thickness of between 0.5 and 1μm is formed on the first silicon oxide layer with a spin-coating method; next, a third silicon oxide layer with a thickness of between 0.2 and 0.5μm is formed on the second silicon oxide layer with a CVD method; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the third silicon oxide layer with a CVD method.

Method 5

**[0072]** A silicon oxide layer with a thickness of between 0.5 and 2μm is formed with a HDP-CVD (High Density Plasma-Chemical Vapor Deposition) method; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxide layer with a CVD method.

Method 6

**[0073]** A USG (Undoped Silicate Glass) layer with a thickness of between 0.2 and 3μm is firstly formed; next, an insulating layer with a thickness of between 0.5 and 3μm, such as TEOS, BPSG (Borophosphosilicate Glass) or PSG (Borophosphosilicate Glass), is formed on the USG layer; and next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the insulating layer with a CVD method.

Method 7

**[0074]** A first silicon oxy-nitride layer with a thickness of between 0.05 and 0.15μm is optionally formed with a CVD method; next, a silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the first silicon oxy-nitride layer with a CVD method; next, a second silicon oxy-nitride layer with a thickness of between 0.05 and 0.15μm is optionally formed on the silicon oxide layer with a CVD method; next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the second silicon oxy-nitride layer or on the silicon oxide layer with a CVD method; next, a third silicon oxy-nitride layer with a thickness of between 0.05 and 0.15μm is optionally formed on the silicon nitride layer with a CVD method; and next, a silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the third silicon oxy-nitride layer or on the silicon nitride layer with a CVD method.

Method 8

**[0075]** A first silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed with a PECVD (Plasma Enhanced Chemical Vapor Deposition) method; next, a second silicon oxide layer with a thickness of between 0.5 and 1μm is formed on the first silicon oxide layer with a spin-coating method; next, a third silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the second silicon oxide layer with a CVD method; next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the third silicon oxide layer with a CVD method; and next, a fourth silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the silicon nitride layer with a CVD method.

Method 9

**[0076]** A first silicon oxide layer with a thickness of between 0.5 and 2μm is formed with a HDP-CVD method; next, a silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the first silicon oxide layer with a CVD method; and next, a second silicon oxide layer with a thickness of between 0.5 and 2μm is formed on the silicon nitride layer with a HDP-CVD method.

Method 10

**[0077]** A first silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed with a CVD method; next, a silicon oxide layer with a thickness of between 0.2 and 1.2μm is formed on the first silicon nitride layer with a CVD method; and next, a second silicon nitride layer with a thickness of between 0.2 and 1.2μm is formed on the silicon oxide layer with a CVD method.

**[0078]** The thickness of the passivation layer 42 is generally more than 0.35μm, and the thickness of the silicon nitride layer is generally more than 0.3μm under an optimal condition.

**[0079]** Refer to Fig.4a. After the passivation layer 42 has been completed, a first polymer layer 46 with a thickness of between 3 and 50μm is formed on the passivation layer 42 and used for insulating. The material of the first polymer layer 46 is thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, or porous dielectric material. The method of forming the first polymer layer 46 includes spin-coating an oligomer film on the passivation layer 42. Refer to Fig.4b. Next, the spun-on oligomer layer 46 with a photosensitive material is patterned with a photolithography method to form multiple openings 48 in the olgomer layer 46 exposing the contact pads 44 on the semiconductor substrate 30. It is to be noted: when the first polymer layer 46 is made of a photosensitive material, it can be patterned with a photolithographic process; when the first polymer layer 46 is made of a non-photosensitive material, it can be patterned with a photolithographic process and an etching process.

**[0080]** Next, the patterned oligomer layer 46 is cured via heating it to the temperature of 200~320℃ with a baking method, a microwave heating method, or an infrared heating method or to the temperature of 320~450℃. The cured first polymer layer 46 has a dimensional

shrinkage and a moisture content less than 1%, which is determined via that the weight variation is less than 1% when the first polymer layer 46 is placed at the temperature of 425~450 ℃. Alternatively, the method of forming the first polymer layer 46 includes: laminating a dry film with a photosensitive material on the passivation layer 42 with a heat-pressing method and then forming openings in the dry film using a photolithography method; or screen-printing an oligomer film on the passivation layer 42 with multiple openings in the oligomer film exposing the contact pads 44, and then curing the oligomer film using a heating process.

**[0081]** Refer to Fig.5. A first adhesion/barrier layer 50 with a thickness of between 400 and 7000Å is formed on the first polymer layer 46 and the contact pads 44 with a sputtering method. The material of the first adhesion/barrier layer 50 is titanium metal, titanium nitride, titanium-tungsten alloy, chromium metal, chromium-copper alloy, tantalum metal, or tantalum nitride. Alternatively, the first adhesion/barrier layer 50 may be a composite of the above-mentioned materials. Next, A seed layer (not shown) with a thickness of between 500 and 5000 angstroms may be formed on the first adhesion/barrier layer 50 using a sputtering process. The seed layer is used to benefit the formation of the succeeding metallic wires; therefore, the material of the seed layer varies with the material to be used by the succeeding metallic wires.

**[0082]** When a copper metallic wire is to be electroplated on the seed layer, copper is a preferable material to the seed layer. When a silver metallic wire is to be electroplated on the seed layer, silver is a preferable material to the seed layer. When a palladium metallic wire is to be electroplated on the seed layer, palladium is a preferable material to the seed layer. When a platinum metallic wire is to be electroplated on the seed layer, platinum is a preferable material to the seed layer. When a rhodium metallic wire is to be electroplated on the seed layer, rhodium is a preferable material to the seed layer. When a ruthenium metallic wire is to be electroplated on the seed layer, ruthenium is a preferable material to the seed layer. When a rhenium metallic wire is to be electroplated on the seed layer, rhenium is a preferable material to the seed layer. When a nickel metallic wire is to be electroplated on the seed layer, nickel is a preferable material to the seed layer.

**[0083]** Refer to Fig.6a. Next, a first patterned photoresist layer 54 is formed on the seed layer on the first adhesion/barrier layer 50. Multiple openings 56 is formed in the first patterned

photoresist layer 54 with a 1X stepper or 1X scanner. The first patterned photoresist layer 54 is a positive photoresist, for example. The openings 56 expose the seed layer on the first adhesion/barrier layer 50. Next, a first metallic layer 58 with a thickness of between 1 and 50μm is electroplated on the seed layer 50 formed on the first adhesion/barrier layer 50 and exposed by the openings 56, and the thickness of the first metallic layer 58 is preferred to be 2~30μm. Thereby, the first metallic layer 58 is electrically connected to the thin-film circuit layers 34. The first metallic layer 58 may be a single layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium, or nickel. Alternatively, the first metallic layer 58 may be a composite of the above-mentioned materials. Next, the first patterned photoresist layer 54 is removed. The first metallic layer 58 is not only simply formed inside the openings 48 but also extended to some portions over the first polymer layer 46. The extended first metallic layer 58 can benefit the formation of the succeeding metal posts.

**[0084]** Next, as shown in Fig.6b, a second patterned photoresist layer 62 is formed on the first metallic layer 58 and the seed layer on the adhesion/barrier layer 50. Multiple openings 64 in the second patterned photoresist layer 62 expose the first metallic layer 58. Next, as shown in Fig.6c, a second metallic layer 66 with a thickness of between 20 and 200μm is formed on the first metallic layer 58 exposed by the openings 64 via electroplating, and the maximum horizontal dimension of each metal post 66 ranges from 3 to 50μm. The second metallic layer 66 serves as metal posts. The material of the second metallic layer 66 may be a single metal layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, rhenium, or nickel. Alternatively, the second metallic layer 66 may be a composite of the above-mentioned materials. The thickness of the second metallic layer 66 is preferred to be 30 to 100microns.

**[0085]** When a second metallic layer 66 of copper is to be electroplated on the first metallic layer 58, copper is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of silver is to be electroplated on the first metallic layer 58, silver is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of palladium is to be electroplated on the first metallic layer 58, palladium is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of platinum is to be electroplated on the first metallic layer 58, platinum is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of

rhodium is to be electroplated on the first metallic layer 58, rhodium is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of ruthenium is to be electroplated on the first metallic layer 58, ruthenium is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of rhenium is to be electroplated on the first metallic layer 58, rhenium is a preferable material to the topmost layer of the first metallic layer 58. When a second metallic layer 66 of nickel is to be electroplated on the first metallic layer 58, nickel is a preferable material to the topmost layer of the first metallic layer 58.

**[0086]** Next, as shown in Fig.6d, the second patterned photoresist layer 62 is removed; next, the seed layer and the first adhesion/barrier layer 50 not under the first metallic layer 58 are subsequently removed using an etching process. If the first adhesion/barrier layer 50 is titanium tungsten alloy, the etchant for etching the first adhesion/barrier layer 50 can be hydrogen peroxide. If the seed layer is gold, the etchant for etching the seed layer is potassium iodide. As shown in Fig.6e, the step of removing the seed layer and the first adhesion/barrier layer 50 not under the first metallic layer 58 may be undertaken before forming the metal Posts 68.

**[0087]** As shown in Fig.7a and Fig.7b, The ratio of the maximum horizontal dimension Hw of the metallic post 66 to the height Ht of the metallic post 66 is less than 4, and the ratio may also be less than 3, 2 or 1. The maximum horizontal dimension of the metallic post 68 is within 3~50microns; therefore, the metallic post 66 is a fine post, which is distinct from the conventional technology. The pitch Hb between the centers of the neighboring metallic posts 68 is 10~250microns, and the preferable spacing Hb is 10~200microns, 10~175microns, or 10~150microns. Fig.7b is a top view showing that the metallic Posts 68 are implemented with the redistribution layer 60 composed of the first adhesion/barrier layer 50 and the first metallic layer 58. From Fig.7b, it can be observed that the metallic post 66 is not formed on the redistribution layer 60 over the openings 48 but formed on the redistribution layer 60 over the first polymer layer 46.

**[0088]** Next, as shown in Fig.8a, a second polymer layer 70 is formed over the semiconductor substrate 30 and covers the metallic Posts 68 and the redistribution layer 60. The material of the second polymer layer 70 may be thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-

Cyclo-Butene), polyurethane, epoxy, parylene polymer, solder-mask material, elastic material, or porous dielectric material. The methods of forming the second polymer layer 70 may include a screen-printing method or a spin-coating method. As shown in Fig.8b, if the second polymer layer 70 is formed with a screen-printing method, multiple openings 72, whereby the top ends of the metallic Posts 68 are revealed, can be formed in the second polymer layer 70 just when screen printing the second polymer layer 70. If the second polymer layer 70 is formed with a spin-coating method, multiple openings 72, whereby the top ends of the metallic Posts 68 are revealed, must be fabricated with a patterning procedure, such as a photolithographic method or a photolithographic method plus an etching method. As shown in Fig.8c, beside via the openings 72, the metallic Posts 68 may also be revealed via a polishing method. However, the second polymer layer 70 needs curing before the polishing procedure. After the second polymer layer 70 has been cured, a CMP (Chemical Mechanical Polishing) procedure or mechanical grinding to polish or grind the second polymer layer 70 is used to reveal the top ends of the metallic Posts 68. The curing procedure may also be undertaken with a baking method, a microwave heating method, or an infrared heating method under the temperature of between 200 and 320 degrees centigrade or between 320 and 400 degrees centigrade.

**[0089]** Here, it is to be stated beforehand that the structures of the following embodiments are predominantly the extensions of the structures shown in Fig.8b and Fig.8c, wherein the metallic Posts 68 has a fine pitch, and the spacing between the centers of the neighboring metallic Posts 68 is within 10~250microns; the ratio of the maximum horizontal dimension of the metallic post 66 Hw to the height of the metallic post 66 Ht is less than 4. The first embodiment is based on the structure illustrated in Fig.8c, and the succeeding embodiments are usually with respect to the variations of the metallic post 66.

**[0090]** Next, as shown in Fig.9, a third polymer layer 74 is formed on the second polymer layer 70 using a spin coating process. Multiple openings 76 are formed in the third polymer layer 74 with a patterning procedure, wherein the patterning procedure is undertaken with a photolithographic method or a photolithographic method plus an etching method. Alternatively, the method of forming the first polymer layer 46 includes: laminating a dry film with a photosensitive material on the passivation layer 42 with a heat-pressing method and then forming openings in the dry film using a photolithography method; or screen-printing an oligomer film on

the passivation layer 42 with multiple openings in the oligomer film exposing the contact pads 44, and then curing the oligomer film using a heating process. The material of the third polymer layer 74 is thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, or porous dielectric material. The metallic posts 68 have a same structure as the previous-mentioned metallic Posts 68. The process for forming the metallic posts 68 is the same as that for forming the previously mentioned metallic Posts 68.

**[0091]** Next, as shown in Fig.10a, a second adhesion/barrier layer with a thickness of between 400 and 7000Å is formed on the third polymer layer 74 and the top ends of the metallic posts 68 with a sputtering method. The material of the second adhesion/barrier layer 78 is titanium metal, titanium nitride, titanium-tungsten alloy, chromium metal, chromium-copper alloy, tantalum metal, or tantalum nitride. Alternatively, the second adhesion/barrier layer 78 may also be a composite of the above-mentioned materials. Next, A seed layer (not shown), such as copper or gold, with a thickness of between 500 and 5000 angstroms may be formed on the second adhesion/barrier layer 78 using a sputtering process. Next, as shown in Fig.10b, a third patterned photoresist layer 82 is formed on the seed layer on the second adhesion/barrier layer 78, wherein the third patterned photoresist layer 82 is a positive-type photoresist. Multiple openings 83 in the third patterned photoresist layer 82 expose the seed layer on the second adhesion/barrier layer 78 over the top ends of the metal posts 68.

**[0092]** Next, as shown in Fig.10c, a third metallic layer 84 is formed on the seed layer on the second adhesion/barrier layer 78 exposed by the openings 83 via electroplating. The third metallic layer 84 may be formed by electroplating a gold layer having a thickness of between 1 and 50 microns on the seed layer, made of gold, exposed by the openings 83. Other materials used to form the third metallic layer 84 may be silver, palladium, platinum, rhodium, ruthenium, or rhenium. Next, as shown in Fig.10d, the third patterned photoresist layer 82 is removed; next, the seed layer and the underlying second adhesion/barrier layer 78 are subsequentially removed. If the second adhesion/barrier layer 78 is titanium tungsten alloy, the etchant for etching the second adhesion/barrier layer 78 can be hydrogen peroxide. If the seed layer is gold, the etchant for etching the seed layer is potassium iodide. It is to be noted that the thickness, material and position of the electroplated third metallic layer 84 is determined by which types of external

devices or circuits are connected to the bumps or pads 84, i.e. the thickness of the third patterned photoresist layer 82, the width of the openings 83 and the position of the openings 83 vary according to the intended application. The abovementioned external circuit may be a flexible circuit board, a semiconductor chip, a printed circuit board, a ceramic substrate, or a glass substrate.

**[0093]** In this embodiment, the third metallic layer 84 may be presented in the form of bumps, contact pads, RDL's, or solder balls. As shown in Fig.10d, when the third metallic layer 84 is a single layer of gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and when the thickness Ha of the third metallic layer 84 is 5~30microns and preferably is 10~25microns, the third metallic layer 84 is defined to be a bump 86. Next, as shown in Fig.11, the semiconductor substrate 30 is diced into multiple semiconductor units 88. The bumps 86 on the semiconductor unit 88 can be electrically connected to an external circuit with ACF (Anisotropic Conductive Film).

**[0094]** Refer to Fig.12a, Fig.12b and Fig. 12c. When the third metallic layer 84 has a solder layer, such as a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy or lead-free solder, and has a thickness Hs of between 20 and 150 microns, and preferably between 30 and 100microns, the semiconductor substrate 30 can be heated to reflow the solder layer of the third metallic layer 84 with the a ball shape, which is defined to be a solder ball 92. The third metallic layer 84 may be formed by electroplating a copper layer having a thickness of between 1 and 100 microns on the seed layer, made of copper, exposed by the openings 83, next electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer exposed by the openings 83, and next electroplating a tin-containing solder layer, such as a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, having a thickness of between 20 and 150 microns on the nickel layer. Next, as shown in Fig.12d, the semiconductor substrate 30 is diced into multiple semiconductor units 88. The solder balls 92 on the semiconductor unit 88 can be electrically connected to an external substrate 94, as shown in Fig. 12e. The external substrate 94 may be a semiconductor chip, a printed circuit board, a ceramic substrate, or a glass substrate. The distance between the centers of the neighboring solder balls 92 may be between 10 and 250 microns.

**[0095]** As shown in Fig.12e, before the solder balls 92 on the semiconductor unit 88 are connected to substrate 94, a fourth polymer layer 96 may be formed on the substrate 94 beforehand. The material of the fourth polymer layer 96 is thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, or porous dielectric material. The fourth polymer layer 96 may be formed on the substrate 94 by laminating a patterned dry film on the substrate 94 using a heat-pressing method, or by laminating a photosensitive dry film on the substrate 94 using a heat-pressing method and patterning the photosensitive dry film with a photolithographic method, or by laminating a non-photosensitive dry film on the substrate 94 using a heat-pressing method and patterning the non-photosensitive dry film with a photolithographic method plus an etching method, or by screen-printing the fourth polymer layer 96 where multiple openings are simultaneously formed in the fourth polymer layer 96, or by spin-coating a photosensitive film on the substrate 94 and then patterning the photosensitive film with a photolithographic method, or by spin-coating a non-photosensitive film on the substrate 94 and patterning the non-photosensitive film with a photolithographic method plus an etching method. After the solder balls 92 on the semiconductor unit 88 are attached to substrate 94, a heating procedure is used to cure the fourth polymer layer 96. The curing procedure is undertaken with a baking method, a microwave heating method, or an infrared heating method.

**[0096]** Refer to Fig.13a and Fig.13b. When the third metallic layer 84 is a single layer made of gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and has a thickness Hp of between 1 and 15microns and preferably between 2 and 10microns, the third metallic layer 84 is defined to be a contact pad 98. The contact pads 98 can be connected to an external circuit with wires formed by a wire bonding process.

**[0097]** Refer to Fig.14a and Fig.14b. When the third metallic layer 84 is made of gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and has a thickness Hr of between 5 and 30microns, and preferably between 10 and 25microns, the third metallic layer 84 may defined to be a metal trace100. The metal trace has a relocated pad connected to the metal post 68, wherein the position of the relocated pad and the metal post 68 connected thereto from a top surface is different. The relocated pad of the metal trace 100 can be connected to an external

circuit with wires formed by a wire-bonding process. The distance between the centers of the wirebonding pads 92 may be between 10 and 250 microns.

**[0098]** In this embodiment, the structures having the bumps, contact pads, RDL's, and solder balls shown in from Fig.9 toFig.14b are all the structures derived from the structure shown in Fig.8c. However, those structures may also be derived from the structure shown in Fig.8b. The structure shown in Fig.9 is fabricated via forming the third polymer layer 74 on the structure shown in Fig.8c and patterning the third polymer layer 74 to form multiple openings in the third polymer layer 74. In the structure shown in Fig.8b, the metallic posts 68 are not revealed via polishing the second polymer layer 70 but revealed via forming multiple openings in the second polymer layer 70 with a patterning procedure. It is unnecessary to form the third polymer layer 74 for the structure shown in Fig.8b. The structure shown in Fig.8b is equivalent to the structure shown in Fig.8c plus the third polymer layer 74. Therefore, the above-mentioned for forming the bumps, contact pads, metal traces, and solder balls derived from Fig. 9, as shown in Figs. 10a-10d, 11, 12a-12e, 13a-13b and 14a-14b, also can be applied to the structure shown in Fig. 8b.

**Embodiment 2**

**[0099]** This embodiment is derived from the structure of Embodiment 1 shown in Fig.8c. As shown in Fig.15a, the top end of the metallic post 68 is a gold layer 102 having a thickness of between 1 and 30 microns, and a wire formed with a wire-bonding process can be connected onto the gold layer 102 of the metallic post 68. It is to be noted: a nickel layer 106 having a thickness of between 1 and 10 microns and a copper layer 104 having a thickness of between 10 and 100 microns and are sequentially below the gold layer 102 to form a copper/nickel/gold structure for the metal post 68. Alternatively, as shown in Fig.15b, a copper layer 104 having a thickness of between 10 and 100 microns is below the gold layer 102 having a thickness of between 1 and 30 microns to form a copper/gold structure for the metal post 68. Alternatively, as shown in Fig.15c, the entire metallic post 68 having a thickness of between 10 and 100 microns may be made of gold.

**Embodiment 3**

**[00100]** This embodiment is derived from the structure of Embodiment 1 shown in Fig.8c. As shown in Fig.16a, a third adhesion/barrier layer 105 is formed on the second polymer layer 70

and on the top end of the metal post 68. The material of the third adhesion/barrier layer 105 is titanium metal, titanium nitride, titanium-tungsten alloy, chromium metal, chromium-copper alloy, tantalum metal, or tantalum nitride. A seed layer (not shown), such as gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, may be sputtered on the third adhesion/barrier layer 105. As shown in Fig.16b, a fourth patterned photoresist layer 110 is formed on the seed layer on the third adhesion/barrier layer 105; a coil-shaped opening 112 in the fourth patterned photoresist layer 110 exposes the seed layer on the adhesion/barrier layer 105. As shown in Fig.16c, a fourth metallic layer 114 is electroplated on the seed layer exposed by the opening 112 in the fourth patterned photoresist layer 110. The fourth metallic layer 114 may be formed by electroplating a single layer of gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, having a thickness of between 1 and 30 microns. Alternatively, the fourth metallic layer 114 may be formed by electroplating a copper layer having a thickness of between 1 and 30 microns, next electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer, and next electroplating a gold layer having a thickness of between 1 and 10 microns on the nickel layer. Preferably, the bottommost metal layer of the fourth metallic layer 114 has a same material as the seed layer. As shown in Fig.16d, the fourth patterned photoresist layer 110 is removed; and next the seed layer and the third adhesion/barrier layer 105 not under the fourth metallic layer 114 are removed. If the third adhesion/barrier layer 105 is titanium tungsten alloy, the etchant for etching the third adhesion/barrier layer 105 can be hydrogen peroxide. If the seed layer is gold, the etchant for etching the seed layer is potassium iodide. As shown in Fig.16e, the fourth metallic layer 114 appears like a coil; thus, the fourth metallic layer 114 is defined to be a first coil-like metallic layer 116. As shown in Fig.16f, the metallic posts 68 electrically connect the first coil-like metallic layer 116 to the semiconductor substrate 30; the first coil-like metallic layer 116 may also be electrically connected to an external circuit via a wire-bonding process; a protection layer 117 having a thickness of between 5 and 25 microns may be formed above the first coil-like metallic layer 116 lest the first coil-like metallic layer 116 be damaged or penetrated by moisture. The material of the protection layer 117 may be an organic or inorganic material or may be thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, porous dielectric material, silicon oxide, compounds of silicon and oxygen, silicate and phosphate glass,

silicon nitride, or silicon oxy-nitride. The first coil-like metallic layer 116 may be used as a passive device, such as an inductor.

**[00101]** The case that the first coil-like metallic layer 116 is applied to an inductor is to be exemplified here. As shown in Fig.16g, a fifth polymer layer 118, such as polyimide or benzo-cyclo-butene (BCB), having a thickness of between 20 and 200microns is formed to cover the first coil-like metallic layer 116. The fifth polymer layer 118 may be formed by spin coating multiple oligomer layers each having a thickness of between 10 and 25 microns or screen-printing a thick oligomer layer. A second coil-like metallic layer 120 is formed on the fifth polymer layer 118 with the same method as that used to form the first coil-like metallic layer 116. The second coil-like metallic layer 120 is electrically connected to an external circuit. When there is a current variation in the external circuit, an electromotive force is induced in the first coil-like metallic layer 116 by the current through the second coil-like metallic layer 120, thereby creating a signal transmitted to the semiconductor substrate 30.

**[00102]** The abovementioned selective electroplating may also be used to form a capacitor element 121 on the second polymer layer 70. As shown in Fig.16h, a low-permittivity layer 121a with a thickness of between 500 and 5000Å is formed on the second polymer layer 70. The material of the low-permittivity layer 121a is titanium metal, titanium-tungsten alloy, tantalum metal, or tantalum nitride, etc. The low-permittivity layer 121a is electrically connected to one of the metallic posts 68. Next, a high-permittivity layer 121b is formed on the low-permittivity layer 121a. The material of the high-permittivity layer 121b is silicon oxy-nitride, silicon oxide, or polyimide. A low-resistance layer 121c is formed on the high-permittivity layer 121b and connected to the other one of the metallic posts 68. The low-resistance layer 121c may be fabricated by sputtering an adhesion/barrier layer, such as titanium, titanium-tungsten alloy, chromium, tantalum or tantalum nitride, having a thickness of between 400 and 7500 angstroms on the high-permittivity layer 121b, next sputtering a seed layer, preferably made of copper, having a thickness of between 500 and 5000 angstroms on the adhesion/barrier layer, next electroplating a copper layer having a thickness of between 1 and 30 microns on the seed layer, next optionally electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer, and next optionally electroplating a gold layer having a thickness of between 1 and 10 microns on the nickel layer or on the copper layer. Alternatively, the low-resistance layer

121c may be fabricated by sputtering an adhesion/barrier layer, such as titanium, titanium-tungsten alloy, chromium, tantalum or tantalum nitride, having a thickness of between 400 and 7500 angstroms on the high-permittivity layer 121b, next sputtering a seed layer, preferably made of gold, having a thickness of between 500 and 5000 angstroms on the adhesion/barrier layer, next electroplating a gold layer having a thickness of between 1 and 30 microns on the seed layer. A protection layer 121d is formed on the low-resistance layer 121c and the second polymer layer 70 lest the capacitor element 121 be damaged. The material of the protection layer 121d may be an organic or inorganic material or may be thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, porous dielectric material, silicon oxide, compounds of silicon and oxygen, silicate and phosphate glass, silicon nitride, or silicon oxy-nitride.

**Embodiment 4**

**[00103]** This embodiment is derived from the structure of Embodiment 1 shown in Fig.8b. As shown in Fig.17a, a fourth adhesion/barrier layer 122, such as titanium, titanium tungsten alloy, chromium, tantalum or tantalum nitride, is formed on the second polymer layer 70 and on the top ends of the metal posts 68 using a sputter process. A seed layer, such as gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, is sputtered on the fourth adhesion/barrier layer 122. As shown in Fig.17b, a fifth patterned photoresist layer 126 is formed on the seed layer on the fourth adhesion/barrier layer 122. A trace-shaped opening 128 in the fifth patterned photoresist layer 126 exposes the seed layer on the fifth patterned photoresist layer 126. As shown in Fig.17c, a fifth metallic layer 130 having a thickness of between 5 and 30microns is electroplated on the seed layer on the fourth adhesion/barrier layer 122 exposed by the opening 128 in the fifth patterned photoresist layer 126; the fifth metallic layer 130 is made of a low-resistance material, such as gold, silver or copper. The fifth metallic layer 130 may be formed by electroplating a single layer of gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, having a thickness of between 1 and 30 microns. Alternatively, the fifth metallic layer 130 may be formed by electroplating a copper layer having a thickness of between 1 and 30 microns, next electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer, and next electroplating a gold layer having a thickness of between 1 and 10 microns on the nickel layer. Preferably, the bottommost metal layer of the fifth

metallic layer 130 has a same material as the seed layer. As shown in Fig.17d, the fifth patterned photoresist layer 126 is removed, and next the seed layer and the fourth adhesion/barrier layer 122 not under the fifth metallic layer 130 are etched away. If the third adhesion/barrier layer 105 is titanium tungsten alloy, the etchant for etching the third adhesion/barrier layer 105 can be hydrogen peroxide. If the seed layer is gold, the etchant for etching the seed layer is potassium iodide.The fifth metallic layer 130 is electrically connected to two metallic posts 68 and functions as the interconnection between multiple metallic posts 68. A protection layer 132 is formed to cover the second polymer layer 70 and the fifth metallic layer 130 lest the fifth metallic layer 130 be damaged or penetrated by moisture. The material of the protection layer 132 may be an organic or inorganic material or may be thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, porous dielectric material, silicon oxide, compounds of silicon and oxygen, silicate and phosphate glass, silicon nitride, or silicon oxy-nitride.

**[00104]** In addition to the fifth metallic layer 130 functioning as the interconnection between the metallic posts 68, multi-layer wire structure may also be fabricated thereby. The metal trace 130 may not be connected up to an external circuitry, but be connected down to transistors or MOS devices. As shown in Fig.17e, a sixth polymer layer 134, such as polyimide or benzo-cyclo-butene (BCB), having a thickness of between 10 and 25 microns is formed on the second polymer layer 70 and on the fifth metallic layer 130. Provided that the metal trace 130 may not be connected up to an external circuitry, but be connected down to transistors or MOS devices, an opening in the sixth polymer layer 134 exposing the metal trace 130 is not necessary. Next, as shown in Fig.17f, the sixth polymer layer 134 is patterned to form multiple openings in the sixth polymer layer 134, whereby the fifth metallic layer 130 is revealed. As shown in Fig.17g, a fifth adhesion/barrier layer 136, such as titanium, titanium tungsten alloy, chromium, tantalum or tantalum nitride, is formed on the sixth polymer layer 134 and on the metal trace 130 with a sputtering method. Next, a seed layer (not shown), such as gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, is sputtered on the fifth adhesion/barrier layer 136. As shown in Fig.17h, a sixth patterned photoresist layer 140 is formed on the seed layer on the fifth adhesion/barrier layer 136, an opening in the sixth patterned photoresist layer 140 expose the seed layer on the fifth adhesion/barrier layer 136. As shown in Fig.17i, a sixth metallic layer 142 is formed on the seed layer exposed by the opening in the sixth patterned

photoresist layer 140. The sixth metallic layer 142 may be formed by electroplating a single layer of gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, having a thickness of between 1 and 30 microns. Alternatively, the sixth metallic layer 142 may be formed by electroplating a copper layer having a thickness of between 1 and 30 microns, next electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer, and next electroplating a gold layer having a thickness of between 1 and 10 microns on the nickel layer. Preferably, the bottommost metal layer of the sixth metallic layer 142 has a same material as the seed layer. As shown in Fig.17j, the sixth patterned photoresist layer 140 is removed; next, the seed layer and the fifth adhesion/barrier layer 136 not under the sixth metallic layer 142 are sequentially removed. As shown in Fig.17k, a seventh polymer layer 144, such as polyimide or benzo-cyclo-butene (BCB), having a thickness of between 10 and 25 microns is formed on the sixth polymer layer 134 and the sixth metallic layer 142. As shown in Fig.17l, the seventh polymer layer 144 is patterned to form multiple openings in the seventh polymer layer 144 exposing the sixth metallic layer 142. As shown in Fig.17m, the revealed sixth metallic layer 142 may be electrically connected to an external circuit with a wire formed by a wire-bonding process, or with a solder bump or gold bump.

**Embodiment 5**

**[00105]** This embodiment is derived from the structure of Embodiment 1 shown in Fig.8b and is similar to Embodiment 4. Refer to Fig.18. The fabrication method of this embodiment is similar to that of Embodiment 4. In Embodiment 4, the fifth metallic layer 130 is made of a low-resistance material and used as a contact pad. However, in Embodiment 5, the seventh metallic layer 146 is made of a high-resistance material, such as chromium-nickel alloy, titanium or tungsten, and is only 1~3microns thick and functions as a resistor element.

**Embodiment 6**

**[00106]** This embodiment is derived from the structure shown in Fig.8a. As shown in Fig.19a and Fig.19.b, in this embodiment, the second polymer layer 70 is removed by first chemical mechanical polishing or mechanical grinding the second polymer layer 70, and then etching the second polymer layer 70 until the top ends and the upper portion of the side walls of the metal posts 68 are revealed. The distance from the top end of the metallic post 68 to the top

surface of the second polymer layer 70 may range from 1 to 150 microns. When the topmost metal layer of the metallic post 68 is gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and the distance from the top end of the metallic post 68 to the top surface of the second polymer layer 70 may range from 15 to 30 microns, the revealed portion of the metallic post 68 may function as a bump. As shown in Fig.19c, thereafter, the semiconductor substrate 30 may be similarly diced into multiple semiconductor units 88. The bumps on the semiconductor unit 88 can be similarly electrically connected to an external circuit with ACF (Anisotropic Conductive Film).

**[00107]** When the topmost metal layer of the metallic post 68 is solder, tin-lead alloy, tin-silver alloy, tin-silver-copper alloy or lead-free solder, and the distance from the top end of the metallic post 68 to the top surface of the second polymer layer 70 may range from 50 to 100 microns, a heating process can be performed to reflow the topmost solder layer of the metallic post 68 to form solder balls after polishing and etching the second polymer layer 70. As shown in Fig.19e, thereafter, the semiconductor substrate 30 may be similarly diced into multiple semiconductor units. Next, the solder balls on the semiconductor unit are electrically connected to an external substrate, and then an eighth polymer layer 148 is filled into the gap between the semiconductor unit and the external substrate and covers every solder balls.

**[00108]** Refer to Fig.19f. When the topmost metal layer of the material of the metallic post 68 is gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and the distance from the top end of the metallic post 68 to the top surface of the second polymer layer 70 ranges from 1 to 10 microns, the revealed metallic post 68 may function as a contact pad. The contact pads can be connected to an external circuit with wires formed by a wire bonding process.

**[00109]** Refer to Fig.19g. When the material of the metallic post 68 is gold, copper, silver, palladium, platinum, rhodium, ruthenium, or rhenium, and the distance from the top end of the metallic post 68 to the top surface of the second polymer layer 70 may range from 5000 angstroms to 10 microns, the revealed metallic post 68 may function as a contact pad. A sixth adhesion/barrier layer 150, such as titanium, titanium-tungsten alloy, chromium, tantalum, or tantalum nitride, having a thickness of between 1000 and 7500 angstroms is formed on the second polymer layer 70 and on the revealed surface of the metallic posts 68. A seed layer (not

shown), such as copper or gold, having a thickness of between 500 and 3000 angstroms is formed on the sixth adhesion/barrier layer 150. As shown in Fig.19h, a seventh patterned photoresist layer 152 is formed on the seed layer on the sixth adhesion/barrier layer 150, and openings in the seventh patterned photoresist layer 152 reveal the seed layer on the sixth adhesion/barrier layer 150. As shown in Fig.19i, an eighth metallic layer 154 is electroplated on the seed layer exposed by the openings in the seventh patterned photoresist layer 152. The eighth metallic layer 154 may be formed by electroplating a single layer of gold, copper, silver, nickel, platinum, palladium, ruthenium, rhodium, or rhenium, having a thickness of between 1 and 30 microns. Alternatively, the eighth metallic layer 154 may be formed by electroplating a copper layer having a thickness of between 1 and 30 microns, next electroplating a nickel layer having a thickness of between 1 and 10 microns on the copper layer, and next electroplating a gold layer having a thickness of between 1 and 10 microns on the nickel layer. Preferably, the bottommost metal layer of the fourth metallic layer 114 has a same material as the seed layer. As shown in Fig.19j, the seventh patterned photoresist layer 152 is removed, and then the seed layer and the sixth adhesion/barrier layer 150 not under the eighth metallic layer 154 are removed The eighth metallic layer 154 interconnects two metallic posts 68 and functions as an interconnection. As shown in Fig.19k, a protection layer 156 is formed to cover the second polymer layer 70 and the eighth metallic layer 154 lest the eighth metallic layer 154 be damaged. The material of the protection layer 156 may be an organic or inorganic material or may be thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, porous dielectric material, silicon oxide, compounds of silicon and oxygen, silicate and phosphate glass, silicon nitride, or silicon oxy-nitride.

**[00110]** Besides, a coil structure, a capacitor structure, a resistor structure, etc. may be connected to the pad formed by polishing and etching the second polymer layer 70 according to the above mentioned process in the embodiment, wherein the distance from the top end of the metallic post 68 to the top surface of the second polymer layer 70 may range from 5000 angstroms to 10 microns.

**Embodiment 7**

**[00111]** The structure of this embodiment is similar to that shown in Fig.8c, but the methods thereof are different for forming the metallic post 68 and the second polymer layer 70. As shown in Fig.20a, after electroplating the first RDL 60, the photoresist layer 54 is removed and the seed layer and the adhesion/barrier layer not under the first RDL 60 are sequentially removed following Fig. 6a. Thereafter, a ninth patterned polymer layer 158 is formed on the first RDL 60 and on the polymer layer 46, and the openings in the ninth patterned polymer layer 158 are 20~200microns deep and expose the first RDL 60.

**[00112]** The material of the ninth patterned polymer layer 158 is thermoplastic, thermosetting plastic, polyimide, BCB (Benzo-Cyclo-Butene), polyurethane, epoxy, parylene-based polymer, solder-mask material, elastic material, or porous dielectric material. The ninth patterned polymer layer 158 is fabricated via heat-pressing a patterned dry film onto the semiconductor substrate 30, or via heat-pressing a photosensitive dry film onto the semiconductor substrate 30 and patterning the photosensitive dry film with a photolithographic method, or via heat-pressing a non-photosensitive dry film onto the semiconductor substrate 30 and patterning the non-photosensitive dry film with a photolithographic method plus an etching method, or via screen-printing the ninth polymer layer 158 where multiple openings are simultaneously formed in the ninth polymer layer 156, or via spin-coating a photosensitive film onto the semiconductor substrate 30 and patterning the photosensitive film with a photolithographic method, or via spin-coating a non-photosensitive film onto the semiconductor substrate 30 and patterning the non-photosensitive film with a photolithographic method plus an etching method.

**[00113]** As shown in Fig.20b, a seventh adhesion/barrier layer 160, such as titanium, titanium-tungsten alloy, chromium, tantalum, or tantalum nitride, having a thickness of between 400 and 7000Å is sputtered on the ninth patterned polymer layer 158, on the first RDL 60 exposed by the openings in the ninth patterned polymer layer 158, and on the side walls of the openings in the ninth patterned polymer layer 158. A seed layer (not shown), such as copper or gold, having a thickness of between 500 and 7500 angstroms is sputtered on the seventh adhesion/barrier layer 160. As shown in Fig.20c, a ninth metallic layer 162 is electroplated with a Damascene method on the seed layer on the seventh adhesion/barrier layer 160 until the ninth metallic layer 162 fills all remaining space in the openings in the ninth patterned polymer layer

158. The ninth metallic layer 162 may be formed by electroplating a copper layer having a thickness of between 1 and 30 microns on the seed layer, preferably made of copper, exposed by the openings in the ninth patterned polymer layer 158. Alternatively, the ninth metallic layer 162 may be formed by electroplating a gold layer having a thickness of between 1 and 30 microns on the seed layer, preferably made of gold, exposed by the openings in the ninth patterned polymer layer 158.

**[00114]** As shown in Fig.20d, the ninth metallic layer 162, the seed layer and the seventh adhesion/barrier layer 160 outside the openings in the ninth patterned polymer layer 158 are removed with a chemical mechanical polishing (CMP) method or a mechanical grinding method. Thereby, the metallic posts 68 are formed. The ratio of the maximum horizontal dimension Hw of the metallic post 68 to the height Ht of the metallic post 68 is less than 4 or even less than 1. The maximum horizontal dimension of the metallic post 68 is 3~50microns; the spacing between the centers of the neighboring metallic posts 68 is 10~250microns.

**[00115]** The metallic post 68 formed with the Damascene method has a similar profile to that disclosed in Fig.8c; therefore, the method to fabricate other elements above the ninth patterned polymer layer 158 and the metallic posts 68 is the same as those formed in the abovementioned embodiments.

**[00116]** Fig.21a through Fig.21d disclose the bumps, contact pads, solder balls and RDL's formed on the ninth patterned polymer layer 158 and the metallic posts 68. Herein, only the completed structures are disclosed; the fabrication methods thereof have been stated in the abovementioned embodiments and will not be described repeatedly.

**[00117]** Fig.22 to Fig.25 disclose the interconnection metal trace, coil, capacitor element, and resistor element formed on the ninth patterned polymer layer 158 and on the metallic posts 68. Herein, only the completed structures are disclosed; the fabrication methods thereof have been stated in the abovementioned embodiments and will not be described repeatedly.

**[00118]** The present invention can apply to release stress and reduce the spacing between metal posts to be less than 250microns. Further, the present invention can increase the pin count to be more than 400. Furthermore, the present invention can greatly reduce the impedance and

loading of the metallic connection circuit of low-power IC elements and then effectively promote the performance of IC elements.

**[00119]** Those embodiments described above are to clarify the present invention to enable the persons skilled in the art to understand, make and use the present invention. However, it is not intended to limit the scope of the scope of the present invention, and any equivalent modification and variation according to the spirit of the present invention is to be also included within the scope of the claims of the present invention stated below.

CLAIMS:

1. A method for fabricating a circuitry component comprising:

providing a semiconductor wafer, a first metal layer over said semiconductor wafer, and a first polymer layer over said first metal layer;

polishing said first polymer layer, wherein said semiconductor wafer is not joined with multiple preformed semiconductor chips having electrical functions before said polishing said first polymer layer;

depositing a second metal layer over said polymer layer and over said first metal layer;

forming a first pattern-defining layer over said second metal layer, an opening in said first pattern-defining layer exposing said second metal layer;

depositing a third metal layer over said second metal layer exposed by said opening in said first pattern-defining layer;

removing said first pattern-defining layer; and

removing said second metal layer not under said third metal layer.

2. The method of claim 1, wherein depositing said first metal layer comprises depositing a first metal post and a second post, wherein the ratio of the greatest transverse dimension of said first metal post to the height of said first metal post is less than 4, and the ratio of the greatest transverse dimension of said second metal post to the height of said second metal post is less than 4, and wherein the distance between the center of said first metal post and the center of said second metal post ranges from 10 microns to 250 microns.

3. The method of claim 1, wherein depositing said first metal layer comprises depositing a gold layer with a thickness of between 20 and 300 microns over said semiconductor wafer.

4. The method of claim 1, wherein depositing said first metal layer comprises depositing a copper layer with a thickness of between 20 and 300 microns over said semiconductor wafer.

5. The method of claim 1, wherein depositing said first metal layer comprises:

depositing a fourth metal layer over said semiconductor wafer;

forming a second pattern-defining layer over said fourth metal layer, an opening in said second pattern-defining layer exposing said fourth metal layer;

depositing a fifth metal layer over said fourth metal layer exposed by said opening in said second pattern-defining layer;

removing said second pattern-defining layer; and

removing said fourth metal layer not under said fifth metal layer.

6. The method of claim 1, wherein said depositing said second metal layer comprises sputtering.

7. The method of claim 1, wherein said depositing said third metal layer comprises electroplating a gold layer with a thickness of between 2 and 50 microns over said second metal layer exposed by said opening in said first pattern-defining layer.

8. The method of claim 1, wherein said depositing said third metal layer comprises electroplating a copper layer with a thickness of between 2 and 30 microns over said second metal layer exposed by said opening in said first pattern-defining layer.

9. The method of claim 1, wherein said depositing said third metal layer comprises electroplating a solder tin-containing layer with a thickness of between 20 and 150 microns over said second metal layer exposed by said opening in said first pattern-defining layer.

10. The method of claim 1, wherein said polishing said first polymer layer until said first metal layer is exposed.

11. The method of claim 1 further comprising forming a second polymer layer over said first polymer layer, wherein said depositing said second metal layer is performed over said second polymer layer and over said first metal layer exposed by an opening in said second polymer layer.

12. The method of claim 1 further comprising forming an opening in said first polymer layer exposing said first metal layer, wherein said forming said opening in said first polymer layer comprises a photolithography process.

13. The method of claim 1 further comprising wirebonding over said third metal layer.

14. A method for fabricating a circuitry component comprising:

providing a semiconductor wafer, a first metal post over said semiconductor wafer, wherein the ratio of the greatest transverse dimension of said first metal post to the height of said first metal post is less than 4, and the height of said first metal post ranges from 20 microns to 300 microns;

forming a first insulating layer over said semiconductor wafer and covering said first metal post, wherein said semiconductor wafer is not joined with multiple preformed semiconductor chips having electrical functions before said forming said first insulating layer;

depositing a first metal layer over said first insulating layer and over said first metal post;

forming a first pattern-defining layer over said first metal layer, an opening in said first pattern-defining layer exposing said first metal layer;

depositing a second metal layer over said first metal layer exposed by said opening in said first pattern-defining layer;

removing said first pattern-defining layer; and

removing said first metal layer not under said second metal layer.

15. The method of claim 14 further comprising providing a second metal post over said semiconductor wafer, wherein the ratio of the greatest transverse dimension of said second metal post to the height of said second metal post is less than 4, and the height of said second metal post ranges from 20 microns to 300 microns, and wherein the distance between the center of said first metal post and the center of said second metal post ranges from 10 microns to 250 microns.

16. The method of claim 14, wherein depositing said first metal post comprises depositing a copper layer with a thickness of between 20 and 300 microns over said semiconductor wafer.

17. The method of claim 14, wherein depositing said first metal post comprises depositing a gold layer with a thickness of between 20 and 300 microns over said semiconductor wafer.

18. The method of claim 14, wherein depositing said first metal post comprises:
depositing a third metal layer over said semiconductor wafer;
forming a second pattern-defining layer over said third metal layer, an opening in said second pattern-defining layer exposing said third metal layer;
depositing a fourth metal layer over said third metal layer exposed by said opening in said second pattern-defining layer;
removing said second pattern-defining layer; and
removing said third metal layer not under said fourth metal layer.

19. The method of claim 14, wherein said depositing said second metal layer comprises electroplating a gold layer with a thickness of between 2 and 50 microns over said first metal layer exposed by said opening in said first pattern-defining layer.

20. The method of claim 14, wherein said depositing said second metal layer comprises electroplating a copper layer with a thickness of between 2 and 30 microns over said first metal layer exposed by said opening in said first pattern-defining layer.

21. The method of claim 14, wherein said depositing said second metal layer comprises electroplating a solder tin-containing layer with a thickness of between 20 and 150 microns over said first metal layer exposed by said opening in said first pattern-defining layer.

22. The method of claim 14 further comprising polishing said first insulating layer until said first metal post is exposed.

23. The method of claim 14 further comprising forming a second insulating layer over said first insulating layer, wherein said depositing said first metal layer is performed over said second insulating layer and over said first metal post exposed by an opening in said second insulating layer.

24. The method of claim 14 further comprising forming an opening in said first insulating layer exposing said first metal layer, wherein said forming said opening in said first insulating layer comprises a photolithography process.

25. A circuitry component comprising:
a substrate;
a first metal post over said substrate, wherein the ratio of the greatest transverse dimension of said first metal post to the height of said first metal post is less than 4, and the height of said first metal post ranges from 20 microns to 300 microns; and
a second metal post over said substrate, wherein the ratio of the greatest transverse dimension of said second metal post to the height of said second metal post is less than 4, and the height of said second metal post ranges from 20 microns to 300 microns, and wherein the distance between the center of said first metal post and the center of said second metal post ranges from 10 microns to 250 microns.

26. The circuitry component of claim 26, wherein the distance between the center of said first metal post and the center of said second metal post ranges from 100 microns to 200 microns.

27. The circuitry component of claim 25 further comprising a first polymer layer over said substrate, wherein said first polymer layer covers said first and second metal posts and has a thickness of between 20 and 300 microns.

28. The circuitry component of claim 25, wherein said first metal post comprises a gold layer with a thickness of between 30 and 100 microns.

29. The circuitry component of claim 25, wherein said first metal post comprises a copper layer with a thickness of between 30 and 100 microns.

30. The circuitry component of claim 25 further comprising a metal trace over said first and second metal posts, wherein said metal trace connects said first and second metal posts.

31. The circuitry component of claim 25, wherein said substrate comprises a semiconductor base, a first metallization structure over said semiconductor base, a passivation layer containing silicon nitride over said first metallization structure, and a second metallization structure over said passivation layer, an opening in said passivation layer exposing a first pad of said first metallization structure, said second metallization structure comprising a second pad connected to said first pad, the position of said first pad from a top view being different from that of said second pad, and said first metal post being over said second pad.

32. The circuitry component of claim 25 further comprising a bump over said first metal post, said bump is used to be joined to a preformed external circuitry, wherein said bump comprises a gold layer with a thickness of between 10 and 30 microns.

33. The circuitry component of claim 25 further comprising a bump over said first metal post, said bump is used to be joined to a preformed external circuitry, wherein said bump comprises a solder tin-containing layer with a thickness of between 20 and 150 microns.

34. The circuitry component of claim 25 further comprising a pad over said first metal post, wherein the greatest traverse dimension of said pad is greater than that of said first metal post, and wherein said pad is used to be wirebonded thereto.

35. The circuitry component of claim 25, wherein said first metal post has a top surface used to be wirebonded thereto.

36. The circuitry component of claim 25 further comprising a metal coil connecting said first and second metal posts.

37. The circuitry component of claim 25 further comprising a metal trace and a bump, wherein said metal trace is over said substrate and said first metal post, said metal trace comprises a pad connected to said first metal post, the position of said pad from a top view being different from that of said first metal post, said bump being over said pad and used to connected to a preformed

external circuitry, wherein said bump comprises a gold layer with a thickness of between 10 and 30 microns.

38. The circuitry component of claim 25 further comprising a metal trace and a bump, wherein said metal trace is over said substrate and said first metal post, said metal trace comprises a pad connected to said first metal post, the position of said pad from a top view being different from that of said first metal post, said bump being over said pad and used to connected to a preformed external circuitry, wherein said bump comprises a solder tin-containing layer with a thickness of between 20 and 150 microns.

39. The circuitry component of claim 25 further comprising a metal trace over said substrate and said first metal post, said metal trace comprises a pad connected to said first metal post, the position of said pad from a top view being different from that of said first metal post, said pad being used to be wirebonded thereto.

40. A circuitry component comprising:

a semiconductor substrate;

a first metal post over said semiconductor substrate, wherein the ratio of the greatest transverse dimension of said first metal post to the height of said first metal post is less than 4, and the height of said first metal post ranges from 20 microns to 300 microns;

a second metal post over said semiconductor substrate, wherein the ratio of the greatest transverse dimension of said second metal post to the height of said second metal post is less than 4, and the height of said second metal post ranges from 20 microns to 300 microns;

a first insulating layer over said semiconductor substrate, wherein said first insulating layer covers said first and second metal posts;

a first bump over said first metal post or over said first insulating layer;

a second bump over said second metal post or over said first insulating layer, wherein the distance between the center of said first bump and the center of said second bump ranges from 10 microns to 250 microns, said first and second bump being used to be joined to a preformed circuitry component.

41. The circuitry component of claim 40, wherein the distance between the center of said first bump and the center of said second bump ranges from 100 microns to 200 microns.

42. The circuitry component of claim 40, wherein said first metal post comprises a gold layer with a thickness of between 20 and 300 microns.

43. The circuitry component of claim 40, wherein said first metal post comprises a copper layer with a thickness of between 20 and 300 microns.

44. The circuitry component of claim 40, wherein said first bump comprises a gold layer with a thickness of between 10 and 30 microns.

45. The circuitry component of claim 40, wherein said first bump comprises a solder tin-containing layer with a thickness of between 20 and 150 microns.

46. The circuitry component of claim 40, wherein said first insulating layer comprises polyimide.

47. The circuitry component of claim 40 further comprises a first metallization structure over said semiconductor substrate, a passivation layer containing silicon nitride over said first metallization structure, and a second metallization structure over said passivation layer, an opening in said passivation layer exposing a first pad of said first metallization structure, said second metallization structure comprising a second pad connected to said first pad, the position of said first pad from a top view being different from that of said second pad, and said first metal post being over said second pad.

48. The circuitry component of claim 40 further comprising a metal trace over said first insulating layer and said first metal post, said metal trace comprising a pad connected to said first metal post, the position of said pad from a top view being different from that of said first metal post, said first bump being over said pad.

49. A method for fabricating a circuitry component comprising:
forming an insulating layer over a substrate, an opening in said insulating layer having a depth of between 20 and 200 microns;
depositing a first metal layer over said insulating layer and in said opening in said insulating layer;
removing said first metal layer outside said opening in said insulating layer;
depositing a second metal layer over said insulating layer and over said first metal layer;
forming a pattern-defining layer over said second metal layer, an opening in said pattern-defining layer exposing said second metal layer;
depositing a third metal layer over said second metal layer exposed by said opening in said pattern-defining layer;
removing said pattern-defining layer; and
removing said second metal layer not under said third metal layer.

50. The method of claim 49, wherein said depositing said first metal layer comprises electroplating a copper layer with a thickness of between 1 and 30 microns over said insulating layer and in said opening in said insulating layer.

51. The method of claim 49, wherein said depositing said first metal layer comprises electroplating a gold layer with a thickness of between 1 and 30 microns over said insulating layer and in said opening in said insulating layer.

52. The method of claim 49, wherein said removing said first metal layer comprises polishing.

53. The method of claim 49, wherein said depositing said third metal layer comprises electroplating a gold layer with a thickness of between 2 and 50 microns over said second metal layer exposed by said opening in said pattern-defining layer.

54. The method of claim 49, wherein said depositing said third metal layer comprises electroplating a copper layer with a thickness of between 1 and 100 microns over said second metal layer exposed by said opening in said pattern-defining layer.

55. The method of claim 49, wherein said depositing said third metal layer comprises electroplating a solder tin-containing layer with a thickness of between 20 and 150 microns over said second metal layer exposed by said opening in said pattern-defining layer.