A METHOD FOR INTEGRATING A SONOS GATE OXIDE TRANSISTOR INTO A LOGIC/ANALOG INTEGRATED CIRCUIT HAVING SEVERAL GATE OXIDE THICKNESSES

ABSTRACT

A method for integrating a SONOS device with an improved top oxide with SiO_2 gate oxides of different thickness is described. In a first embodiment during ISSG oxidation to form the SiO_2 gate oxides, a thin sacrificial silicon nitride layer is used over the top oxide of the ONO to minimize loss and to control the top oxide thickness. In a second embodiment the top oxide layer for the SONOS device is formed by depositing an NO stack. During ISSG oxidation to form the SiO_2 gate oxides a portion of the Si_3N_4 in the NO stack is converted to SiO_2 to form the top oxide with improved thickness control.

FIG 8.