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UV AND REDUCING TREATMENT FOR K RECOVERY AND SURFACE CLEAN IN SEMICONDUCTOR PROCESSING

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Patent Application No. 61/260,789 filed November 12, 2009, titled UV AND REDUCING TREATMENT FOR K RECOVERY AND SURFACE CLEAN IN SEMICONDUCTOR PROCESSING and U.S. Utility Patent Application No. 12/646,830 filed December 12, 2009, titled UV AND REDUCING TREATMENT FOR K RECOVERY AND SURFACE CLEAN IN SEMICONDUCTOR PROCESSING. These patent applications are incorporated herein by reference in their entirety for all purposes.

BACKGROUND OF THE INVENTION

[0002] The invention relates to semiconductor processing, in particular to surface cleaning and repair of process-induced damage of low dielectric constant dielectric materials in, for example, damascene processing.

[0003] Low dielectric constant (low-k) insulating materials have been integrated into semiconductor devices in order to address reduced feature sizes and high performance requirements. These low-k dielectrics are mechanically weaker than previous generation dielectric materials. The inherently weak nature of the low-k dielectric material can pose significant challenges for downstream electronic-packaging processes and material compatibility.

[0004] Low-k materials are, by definition, those semiconductor-grade insulating materials that have a dielectric constant ("k") lower than that of SiO₂, i.e., 3.9. Various types of low-k materials can have dielectric constants ranging from about 3.8-3.6 (e.g., fluorosilicate glass (FSG)), to less than about 3.2 (e.g., (carbon doped oxide (CDO)), to as low as 2.2 (e.g., spin-on glass (SOG)) or even lower, and encompass low-k dielectrics referred to as "ultra low-k" (ULK) and "extreme ultra low-k" (ELK). In many CDO low-k implementations, such as are described herein as one aspect of the invention, suitable carbon-containing low-k materials have a dielectric constant of about 2.7 or lower. To further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and insulators having low dielectric constants to reduce the capacitive



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coupling between adjacent metal lines. Low-k materials are being integrated into the devices to improve device performance and allow for device scaling.

[0005] Low-k materials are less dense than standard insulating materials such as SiO_2 . This low density introduces a host of process integration and material compatibility difficulties. Achieving a balance between maintaining a low-k film's integrity, integrating it properly, and performing the necessary stripping, cleaning, and conditioning is challenging. Patterning processes (etching, stripping, deposition, and cleaning) can also have a drastic impact on the integrity of carbon-containing low-k materials, in particular SiOC-based low-k materials.

[0006] The properties that give carbon-containing low-k dielectric materials their desirable low dielectric constants are the very same properties that are leading to significant integration challenges. Carbon-containing low-k materials achieve lower dielectric constants through the incorporation of non-polar covalent bonds (e.g., from the addition of carbon) and the introduction of porosity to decrease film density. Introducing porosity or the incorporation of terminal bonds, such as Si-CH_3 , breaks the continuity of the rigid Si-O-Si lattice of traditional oxides, yielding a lower dielectric constant film that is both mechanically and chemically weaker. Because of the mechanical weakness, carbon-containing low-k films are susceptible to kinetic plasma damage that can undesirably densify the film and thus increase the film's effective k value.

[0007] Furthermore, chemical plasmas used in semiconductor processing operations to which dielectrics are exposed can modify carbon-containing low-k films where bonds such as Si-CH_3 are readily broken. The susceptibility of carbon-containing low-k materials to plasma modification poses a serious integration challenge since plasma processes are routinely used to etch, clean, and deposit films in the manufacturing of a semiconductor device. In a typical Damascene process flow, prior to metal barrier deposition, process induced carbon-containing low-k dielectric damage can be incurred by a patterned low-k dielectric from (plasma) etch, dry resist strip, wet cleaning and dry cleaning. Carbon-containing low-k materials are also susceptible to the intercalation of plasma species, residues, solvents, moisture, and precursor molecules that can either adsorb into, outgas from, or chemically modify the film. Thereafter, a conductive material, typically a metal, for example copper, is deposited onto the patterned dielectric layer to fill vias and trenches formed

in the dielectric layer. Then, excess metal is removed via chemical mechanical polishing (CMP), thereby forming a planar surface comprising regions of exposed copper and low-k dielectric onto which other layers, such as a dielectric barrier, are deposited. The CMP process typically damages the low-k dielectric, resulting in carbon loss and water absorption. This causes the k of the low-k dielectric to increase, thereby lowering the RC improvement that the low-k material can potentially provide.

[0008] Also, exposed metal, particularly copper, regions are subject to oxidation prior to the formation of a dielectric barrier or subsequent layers on the wafer surface. And, organic residues of anti-corrosion components of CMP slurry, for example benzotriazole (BTA), may remain on a wafer surface after a CMP process. The presence of copper oxide and organic residue causes problems with the adhesion of the dielectric barrier on the wafer surface. Therefore, various cleaning processes may be used to remove such oxide and residue (another form of process-induced damage). In one specific example, such a wafer may be exposed to a direct plasma in a plasma-enhanced chemical vapor deposition (PECVD) processing chamber for a period of time prior to introducing chemical vapors to the processing chamber. The use of a reducing plasma, such as an ammonia or hydrogen plasma, may reduce copper oxide and hydrocarbons on the surface, thereby cleaning the surface. However, depending upon processing conditions, such direct plasmas also may affect a low-k dielectric surrounding the copper because the low-k material is locally densified at the surface either by ion bombardment or because of bound carbon removal through chemical activity. Some of the k damage induced by operations such as CMP to the low-k material may be recovered by doing a short anneal prior to the above described pre-treatment and etch stop deposition, but the recovery is only marginal.

SUMMARY OF THE INVENTION

[0009] The present invention provides a method for treatment of carbon-containing low-k dielectric, for example, but not limited to carbon-doped oxide (CDO), and possibly including a metal feature, with a reducing agent and ultraviolet (UV) radiation, for the repair of process-induced damage. In another aspect, treatment with a reducing agent and ultraviolet (UV) radiation is effective to clean a processed wafer surface by removal (reduction) of metal oxide (e.g., copper oxide) and/or organic residue of CMP slurry from the planarized surface of a processed

wafer. The methods of the invention are particularly applicable in the context of damascene processing to recover lost low-k property of a dielectric damaged during processing, either pre-metalization, post-planarization, or both, and/or provide effective post-planarization surface cleaning to improve adhesion of subsequently applied dielectric barrier and/or other layers.

[00010] In one embodiment, the invention involves exposing a patterned metal (e.g., copper) interconnect wafer (post-CMP and prior to etch stop deposition) to a sufficient flux of ultraviolet (UV) radiation and a reducing agent, such as NH_3 , resulting in metal oxide (e.g., copper oxide) reduction and removal of adsorbed organic residue remaining after CMP with minimal impact on the dielectric constant of the exposed dielectric (which may be low-k, for example a carbon-containing, e.g., CDO, such as ULK; or other low-k or non-low-k dielectric). This pre-treatment in and by itself can also recover some of the damage imparted to a low-k dielectric at the substrate surface (e.g., k degradation due to absorbed water). There are several other possible approaches in accordance with the invention such as the use of a short anneal (e.g., 1 minute or less) involving exposure of the dielectric surface to a reducing agent at a temperature of about 400°C , followed by a short UV exposure in an inert atmosphere such as Helium. In another embodiment, the wafer is exposed to UV in a reducing atmosphere, such as NH_3 , to clean the metal (e.g., copper) surface, followed by UV exposure in an inert atmosphere for k damage recovery. In either case, the measured recovery of dielectric constant is more than what an anneal can achieve on its own.

[00011] While reduction of copper oxide is a particularly useful and exemplified embodiment, in other embodiments this same approach can be applied to the reduction of nickel oxide, tungsten oxide, cobalt oxide, or other metal oxides prior to dielectric and/or metallic barrier deposition, contact formation, or similar deposition process.

[00012] This process is amenable to inclusion on a properly designed load lock or as a module for a PECVD semiconductor wafer processing system, such as a Vector Extreme configured PECVD system, available from Novellus Systems, Inc., San Jose, CA, for example.

[00013] In another aspect, the invention relates to a method of forming a semiconductor device. The method includes receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric layer having formed therein a feature, the feature having sidewalls and a bottom; and exposing the feature to a reducing agent and UV radiation. The process induced low-k dielectric damage in the feature is repaired.

[00014] In another aspect, the invention relates to a method of forming a semiconductor device involving receiving in a processing chamber a semiconductor device substrate comprising a planarized surface having conductive features in a dielectric layer; and exposing the planarized surface to UV radiation and a reducing agent. Planarization-induced damage on the surface is repaired.

[00015] The invention may also be more generally applicable in other semiconductor processing contexts. For example, receiving in a processing chamber a semiconductor device substrate, and exposing the semiconductor device substrate to UV radiation and a reducing agent such that processing-induced damage to the semiconductor device substrate is repaired.

[00016] These and other features and advantages of the present invention will be described in more detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[00017] Figure 1 is a process flow chart depicting a method in accordance with an embodiment of the invention.

[00018] Figures 2A-2D are cross-sectional diagrams illustrating the formation of a semiconductor device by a dual damascene process in accordance with an embodiment of the invention.

[00019] Figure 3 is a schematic diagram of an example chamber suitable for implementing the present invention.

[00020] Figures 4-8 provide data plots illustrating the benefits of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[00021] Embodiments of the present invention are described herein primarily in the context of a treatment for carbon-containing low-k dielectric repair in damascene

processing. Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings.

[00022] The term “semiconductor device” as used herein refers to any device formed on a semiconductor substrate or any device possessing a semiconductor material. In many cases, a semiconductor device participates in electronic logic or memory, or in energy conversion. The term “semiconductor device” subsumes partially fabricated devices (such as partially fabricated integrated circuits) as well as completed devices available for sale or installed in particular apparatus. In short, a semiconductor device may exist at any state of manufacture that employs a method of this invention or possesses a structure of this invention.

[00023] As noted above, the present invention provides a method of semiconductor device fabrication that involves exposure to a reducing agent and UV radiation. Treatments in accordance with the invention are effective for the repair of process-induced damage to the dielectric, for example, broken Si-CH₃ bonds in carbon-containing low-k dielectric (e.g., CDO) resulting from plasma trench etching, or oxidized metallization or organic residue resulting from CMP. Applicable carbon-containing dielectrics typically have SiO-based backbones doped with carbon, in particular CDO (for example, those formed from octamethyl cyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TMCTS), dimethyldimethoxysilane (DMDMOS), and diethoxymethylsilane (DEMS) and other known CDO precursors), but may also include hybrid polymers incorporating both C, Si and O in the backbone. The invention is applicable, at least in its post-planarization damage repair (e.g., surface cleaning) aspect to semiconductor substrates having non-carbon-containing low-k dielectrics, or non-low-k dielectrics at all, since the metal oxide reduction and organic CMP residue removal aspects are independent from the low-k dielectric repair and k-recovery aspect of the invention. The inventive methods are particularly applicable in the context of damascene processing.

[00024] In one aspect, the invention relates to a method of forming a semiconductor device by exposing a feature formed in a carbon-containing low-k

dielectric layer to a reducing agent and UV radiation, either simultaneously or successively, to repair process induced low-k dielectric damage (e.g., dangling bonds or highly strained bonds, e.g., Si-O-Si or Si-CH₂-Si, caused by removal of organic (generally -CH₃) groups) to the low-k material of the feature sidewalls and bottom caused by plasma etch, dry resist strip, wet cleaning and dry cleaning, for example, involved in the feature formation process. The repaired feature can then be filled with a conductive material, particularly a metal diffusion barrier, followed by copper (or other suitable interconnect metal). The top surface of the semiconductor device can then be planarized, generally by chemical mechanical polishing (CMP). As noted above, post-planarization repair of planarization-induced dielectric damage in addition to or independent from pre-metallization dielectric repair are aspects of the invention.

[00025] Figure 1 is a process flow chart depicting operations that may be performed in various methods in accordance with embodiments of the present invention. The invention is advantageously applied in a damascene processing context, although its application is not so limited. It should be understood that, in at least some aspects, the present invention requires only the UV radiation and reducing agent exposure of an applicable semiconductor device substrate such as described in operations 104 and/or 110 of the embodiment illustrated in Figure 1. Other aspects of the invention may include additional processing operations, such as damascene processing operations described herein. But the invention is not limited to the performance of these additional processing operations in all its aspects. A generalized version of a dual damascene technique is described below with reference to Figures 2A through 2D, which depict a partially formed semiconductor device during various stages of this process. The invention may also be used in conjunction with other semiconductor processing techniques.

[00026] Referring now to Figure 1, in operations that are not necessarily part of the present invention, but place an embodiment of the invention in context in an advantageous application, a carbon-containing low-k dielectric layer is deposited on a substrate at 100. Patterns of conductive features are formed in the dielectric layer, generally by plasma etching, at 102. Plasma etching generally results in damage to the pattern edges, generally trench sidewalls and bottoms, as described above. Other process operations, such as dry resist strip, wet cleaning and dry cleaning, can also

cause or contribute to low-k dielectric damage. The conductive features are typically, though not necessarily, metal lines and vias. In one example, they are the interconnects of a metallization layer that is formed from copper. As is known to those of skill in the art, various techniques may be employed to form such layers.

[00027] The formed features (e.g., etched trenches) are then exposed to a reducing agent and ultraviolet (UV) radiation at 104. While the invention is not limited to any particular theory of operation, it is believed that the UV exposure of the damaged dielectric surface according to this aspect of the invention cross-links the surface Si groups to fill gaps from the departed methyl ($-CH_3$) groups. In addition, the UV energy may photo-excite the reducing agent to produce hydrogen or hydrogen-like (e.g., Deuterium) radicals which in turn volatilize and remove or react away certain dangling bonds or non-structure forming carbon components which otherwise increase the polarizability of the matrix thus increasing the dielectric constant. In some embodiments, this reducing agent-mediated aspect of the low-k dielectric repair may involve exposure of the dielectric to a silylating agent, such as hexamethyldisilazane (HMDS) prior to or during the UV exposure, as described further below.

[00028] The reducing agent is typically a reducing gas, and may be photoactive either alone or in combination with other chemical species present in the processing chamber. Suitable examples of reducing agents include NH_3 , or NH_3 -like compounds, wherein the H is replaced by deuterium (e.g., NH_2D , NHD_2 , ND_3), H_2 ; hydrazine (N_2H_4), or other photoreactive gases that can produce a H- radical such as tetramethylsilane (4MS) or trimethylsilane (3MS), amines (e.g., methyl-, dimethyl- or trimethyl- amine, or ethylamine), alkenes such as ethylene or propylene, or alkynes such as acetylene, or combinations of these with one another and/or inert gases such as He, N_2 or Ar. In specific examples, the reducing gas may be NH_3 or H_2 . A specific example is NH_3 .

[00029] According to various embodiments of the invention, the feature may be exposed to UV radiation in the presence of the reducing agent. In other embodiments, the feature may be exposed to UV radiation following exposure to the reducing agent, for example an initial anneal or soak of the feature with a reducing gas (e.g., NH_3), for example at a temperature below the targeted thermal budget, for example about $400^\circ C$, for about 30 seconds, followed by UV exposure in an inert gas (e.g., He), for

example for about 30 seconds. In still other embodiments, an initial exposure to UV radiation in the presence of the reducing agent can be followed by a further exposure to UV radiation without the reducing agent, for example in an inert gas (e.g., He); or the reverse operations (i.e., exposure to UV radiation without the reducing agent, for example in an inert gas (e.g., He) followed by a further exposure to UV radiation in the presence of the reducing agent.

[00030] In another embodiment, damaged dielectric can be exposed to a silylating agent, such as HMDS, for example at a temperature of about 400°C (anneal), followed by or during exposure to UV radiation, either in the presence of a reducing agent, such as NH₃, or an inert gas like He, Ar or N₂ where, for example, the substrate has previously been exposed to a reducing agent.

[00031] Following the treatment, a barrier layer may be deposited on the low-k dielectric layer, prior to subsequent processing of the semiconductor device.

[00032] Suitable reducing agent partial pressures are between about 1 and 700 Torr, for example 50-600 Torr. A typical reducing agent flow rate is about 15 slm. Exposure times of less than a minute, for example 30 or 25 seconds, are generally suitable. At very lower partial pressures, longer exposure times will generally be required.

[00033] The UV radiation may be obtained from any suitable UV source. The choices of UV wavelength(s), total exposure time and intensity, etc., depend on a number of factors, including the thickness of the dielectric film and the composition of the dielectric film. Suitable UV treatment parameters are in the power intensity range of about 1 mw- 20W/cm², preferably about 500mW-5W/cm²; at a wavelength of about 150-500nm, preferably about 200-400nm; for up to about 1 minute, for example about 15, 30 or 45 seconds; at a wafer temperature of between room temperature up to about 450°C, preferably about 200-400°C. A typical UV exposure in accordance with this aspect of the invention has a power density of about 1-3 W/cm² at a wafer temperature of about 400°C for about 30 seconds. The UV source can be a single wavelength excimer lamp or broad spectrum source with arc or microwave excitations. The process pressure can range from about 1mTorr to 760 Torr, preferably from about 5 Torr to 700 Torr.

[00034] In one particular implementation on a SOLA UV thermal processing system, available from Novellus Systems, Inc., UV intensity can be anywhere between 10-100%. Lower intensity generally requires longer exposure times, particularly for cleaning. Temperature is set below target thermal budget (e.g., 350-400°C). Pressure can be as noted above. The UV wavelength used can be a broad band source using H⁺ bulbs with wavelength lower than 230nm since NH₃ absorbs in this region. Other sources that produce such short wavelengths such as 172nm excimers can also be used.

[00035] The process parameters for the UV treatment, including intensity, wavelength, temperature, pressure, time and gas flow, may be independently controlled and varied, and any or all of the process conditions may be varied from station to station where the invention is implemented in a multi-station processing apparatus. In particular, there may be independent control of temperature, reducing agent and UV irradiation. For example, the wafer may be brought to a temperature T for a time t, exposed to a reducing agent for a time t₁, exposed to UV radiation and a reducing agent for time t₂, exposed to UV radiation only for a time t₃, and then moved to another station in a multi-station processing apparatus where any of the conditions including temperature, UV radiation intensity, pressure, wavelength, flow, and time may be independently changed within the described parameters.

[00036] The apparatus employed to implement the invention can have one or more UV sources. In some embodiments described herein, the apparatus will have a single UV source. Suitable apparatus are described in more detail below.

[00037] Following this UV treatment, in operations that are not necessarily part of the present invention but are provided for context for one embodiment as noted above, the trenches may then be filled at 106 with a conductive material, typically copper (Cu), although other metals may also be used. When filling the features, excess material will have to be removed from the top (exposed surface) of the dielectric layer. The excess material may be removed by a planarization process to form an exposed pattern of conductive features in the dielectric at 108. As discussed above, one widely-used planarization process is chemical mechanical polishing (CMP).

[00038] CMP slurry oxidizes the surface of the conductive material during planarization. It is beneficial to remove oxides from the conductive material after the planarization process. As discussed above, slurry from CMP can chemically remove carbon groups from the dielectric as well. In addition, organic residues of anti-corrosion components of CMP slurry, for example benzotriazole (BTA), may remain on a wafer surface after a CMP process. The presence of copper oxide and organic residue can interfere with the adhesion of subsequently applied layers, such as a dielectric barrier, on the wafer surface.

[00039] According to a further aspect of the invention, to repair the dielectric and remove the metal oxide and/or CMP slurry organic residue, the dielectric surface can be exposed to a further reducing agent and UV radiation treatment at 110. The treatment may be conducted under the same conditions as described above with reference to the post-trench etch treatment. The UV and reducing agent exposure of the present invention is also effective for removing metal oxide and CMP organic residue. While the invention is not limited to any particular theory of operation, it is believed that the UV exposure of the planarized surface according to this aspect of the invention cross-links the surface Si groups to fill gaps in the low-k dielectric from departed methyl ($-CH_3$) groups. In addition, the UV energy may photo-excite the reducing agent to produce hydrogen (or hydrogen-like) radicals which in turn volatilize and remove or react away certain dangling bonds or non-structure forming carbon components which otherwise increase the polarizability of the matrix thus increasing the dielectric constant, and also volatilize and remove or react away CMP organic residue. In addition, hydrogen (or hydrogen-like) radicals produced which can in turn drive the reduction of copper oxide to pure copper.

[00040] Following the damascene processing repair in accordance with the present invention, a diffusion barrier film, such as a copper diffusion barrier film, may be deposited on the planarized surface of the partially-formed semiconductor device. This layer may serve other purposes aside from that of a diffusion barrier. For example, the diffusion barrier film may also act as an etch stop layer.

[00041] According to various implementations of the present invention, a reducing agent and UV exposure treatment, as described above, may be conducted at either or both the pre-metallization (e.g., trench fill) and post-planarization stages of a semiconductor processing operation. The operation may include either or both

processing operations. In embodiments where the reducing agent and UV exposure treatment is not applied at both stages of a semiconductor processing operation that includes both pre-metallization and post-planarization processing, other processing techniques may be combined with the reducing agent and UV exposure treatment at one stage or the other. For example, a UV exposure without reducing agent exposure may be used at one stage or the other.

[00042] Further, other processing operations may be combined with the reducing agent and UV exposure treatment at a given processing stage. For example, one embodiment of the invention involves a two-step post-CMP stage process involving dielectric repair for k recovery with UV cure in an inert (e.g., He) atmosphere, followed by UV cure with a reducing agent (e.g., NH_3) for surface cleaning; or the steps may be reversed. According to these embodiments, a short anneal (e.g., 30 seconds at 400°C) before or after UV cure in NH_3 enables both surface cleaning and k recovery in a single treatment.

[00043] Referring now to Figures 2A-2D, a typical dual damascene process incorporating processing-induced damage repair processes of the present invention is illustrated. As noted above, it should be understood that an embodiment of the invention in context in an advantageous application is depicted. In at least some aspects, the present invention requires only the UV radiation and reducing agent exposure of the semiconductor device substrate, as described above. Other aspects of the invention may include additional processing operations, such as damascene processing operations described herein. But the invention is not limited to the performance of these additional processing operations in all its aspects.

[00044] Referring to Figure 2A, first 203 and second 205 layers of dielectric are deposited in succession, possibly separated by deposition of an etch stop layer, such as a silicon nitride layer. As is well known in the art, according to alternative damascene processing techniques a single thicker dielectric layer can be used instead of discrete first and second layers.

[00045] After deposition of the second dielectric layer 205, a via mask 211 is formed having openings where vias will be subsequently etched. Next, the vias are partially etched down through the level of the second dielectric 205. Then via mask 211 is stripped off and replaced with a line mask 213 as depicted in Figure 2B. A

second etch operation is performed to remove sufficient amounts of dielectric to define line paths 215 in second dielectric layer 205. The etch operation also extends via holes 217 through first dielectric layer 203, down to contact an etch stop layer 210 above a metal layer 211 on the underlying substrate 209.

[00046] It should be noted that the foregoing description is just an example of one dual damascene process with which the present invention may be implemented. One type of via-first dual damascene process has been described. In other embodiments, a via-first process may involve complete etching of the vias prior to etching of the line trenches. Or, a trench-first process, in which the etching of the line trenches precedes the via etching, may be used. These various damascene processing techniques, and other variations thereon, are well known in the art and represent alternative implementation contexts for embodiments of the present invention. The invention is also applicable to single damascene processing, more conventional metal deposition and etch, contact cleaning, and essentially any semiconductor processing context where carbon-containing low-k dielectrics are used (for the low-k repair aspect of the invention) and/or, for at least the post-planarization aspect of the invention, any semiconductor context in which metal oxide reduction or removal of organic CMP residue (surface cleaning) is required. In the case of contact cleaning, it should be understood that the metal oxide reducing aspect of the invention has two variants in a contact cleaning process, either or both of which may be performed in accordance with the present invention: Cleaning of the etched contact via prior to metal deposition and cleaning the filled metal contact after chemical mechanical polishing (CMP). In the first instance, the UV and reducing agent treatment reduces the oxide created in a silicide such as NiSi. In the second instance, the treatment reduces metal oxide grown on top of the metal contact, generally on metals such as W or Cu.

[00047] Further in this regard, the term "trench" in the context of damascene processing is commonly understood to describe a feature formed in dielectric and subsequently filled to form a conductive line in a dielectric layer. In a more general semiconductor processing context, the term is also understood to describe a feature formed in dielectric and subsequently filled to form an element of a semiconductor device (e.g., via, line, STI, etc.), and may include a damascene trench or a combined

damascene structure. Unless it is otherwise clear from the context, when used herein, the term should be understood to have its broader meaning.

[00048] After trench etching, the photoresist is removed in another plasma process, followed by a wet or dry clean and then damage on the low-k dielectric surface is repaired, as discussed above.

[00049] Thereafter a thin layer of conductive barrier layer material 219 is formed on the exposed surfaces (including sidewalls) of dielectric layers 203 and 205. Conductive barrier layer material 219 may be formed, for example, of tantalum or tantalum nitride. A CVD or PVD operation is typically employed to deposit conductive barrier layer material 219. Prior to the deposition of the barrier material, a plasma process is typically used to clean the bottoms of the trenches to remove oxidation and contaminants from the exposed copper surface on the underlying layer. As is known to those skilled in the art, this barrier “preclean” plasma process can be simply an inert plasma or a reactive plasma of a gas such as hydrogen. The preclean plasma process can also damage a low-k dielectric film. A reducing agent and UV treatment as described above to repair the damaged low-k film may be employed prior to the PVD operation- for Ta or TaN.

[00050] On top of the barrier layer, a conductive metal (typically copper) is deposited in the trench and line paths 217 and 215. Conventionally this deposition is performed in two steps: an initial deposition of a conductive seed layer followed by bulk deposition of copper by electroplating. The seed layer may be deposited by physical vapor deposition, chemical vapor deposition, electroless plating, etc. Note that the bulk deposition of copper not only fills line paths 215 but, to ensure complete filling, also covers all the exposed regions on top of second dielectric layer 205.

[00051] Thus, it becomes necessary to planarize the structure and remove the excess copper from the device. Planarization removes material down to the level of the top of dielectric layer 205. This results in an exposed pattern of conductive lines 221 in dielectric layer 205 and vias in dielectric layer 203. (See the cross-sectional view of Figure 2C and the simplified top view of Figure 2D.)

[00052] Planarization may be accomplished by various techniques. Typically, the process involves some amount of CMP. It may also involve a combination of electropolishing, to remove most of the excess bulk copper, followed by CMP to

remove the remaining copper down to the level of the top surface of dielectric layer 205. As discussed above, slurry from CMP can chemically remove carbon groups, and the in-situ plasma based processes typically used to remove the oxides from the conductive lines after the planarization process can also remove carbon groups leaving silicon dangling bonds on the surface of low-k dielectric films. Each of these types of damage also results in significant water absorption, resulting in an increase in dielectric k.

[00053] As described previously, another aspect of the invention relates to post-planarization (e.g., CMP) damage repair arising in damascene processing. According to this aspect, following planarization by CMP, Si-OH (silanol) bonds (formed by removal of organic (generally $-CH_3$) groups by CMP slurry and processing and reaction of water in the slurry with resulting dangling Si- bonds), or other carbon-containing low-k dielectric film damage (e.g., highly strained bonds), or metal oxidation or CMP slurry organic residue contamination are repaired by exposing the surface to a reducing agent and UV radiation, as described above.

Apparatus

[00054] The present invention can be implemented in many different types of apparatus. In some embodiments, the apparatus will include one or more chambers (sometimes referred to as process modules) that house one or more wafers and are suitable for wafer processing. At least one chamber will include a UV source. A single chamber may have one or more stations and may be employed for one, some or all operations of the invention. Each chamber may house one or more wafers (substrates) for processing. The one or more chambers maintain the wafer in a defined position or positions (with or without motion within that position, e.g., rotation, vibration, or other agitation) during procedures of the invention. For certain operations in which the wafer temperature is to be controlled, the apparatus may include a controlled temperature wafer support, which may be heated, cooled, or both. The wafer support may also be controllable to provide the defined wafer positions within a process module. The wafer support may rotate, vibrate, or otherwise agitate the wafer relative to the UV source.

[00055] Figure 3 depicts the arrangement of a UV light source suitable for implementation of the present invention. In this embodiment, a cold mirror reflector

seeks to diminish the incidence of IR radiation on the wafer, while permitting UV radiation to be available for processing. For clarity, this figure depicts only one of the possible multiple processing stations available in an apparatus of this invention. Also, this figure omits depiction of the wafer for purposes of clarity, and shows a flood-type reflector. It will be apparent to those skilled in this art that the principles depicted in Figure 3 may also be applied to a focused reflector.

[00056] Referring to Figure 3, pedestal 303 is embedded into one station of a processing chamber 301. Window 305 is located appropriately above pedestal 303 to permit radiation of the wafer (not shown here) with UV output of the desired wavelengths from UV lamps 309 and 319. Suitable lamps for the UV light source may include, but are not limited to, mercury vapor or xenon lamps. Other suitable light sources include deuterium lamps, excimer lamps or lasers (e.g., excimer lasers and tunable variations of various lasers). Both lamps 309 and 319 are equipped with reflectors 307 and 317 which render their output into flood illumination. Reflectors 307 and 317 may themselves be made from "cold mirror" materials, i.e., they may also be designed to transmit IR and reflect UV radiation.

[00057] Radiation emanating directly from lamps 309 and 319 as well as that reflected from reflectors 307 and 317 is further incident upon a set of reflectors 311. These reflectors are also cold mirrors designed to reflect only those UV wavelengths that are desired for the purposes of curing the film on the wafer. All other radiation including visible and most particularly the IR is transmitted by this set of cold mirrors. Therefore the wafer is radiated only by those wavelengths that cause the desired effect on the film. It will be apparent to those skilled in this art that the specific angle, distance, and orientation of the cold mirror reflectors 311 with respect to the lamps 309 and 319 may be optimized to maximize the UV intensity incident on the wafer and to optimize the uniformity of its illumination.

[00058] The chamber 301 is capable of holding a vacuum and/or containing gases at pressures above atmospheric pressure. For simplicity, only one station of one chamber 301 is shown. It is noted that in some embodiments, chamber 301 is one chamber in a multi-chambered apparatus, although chamber 301 could alternatively be part of a stand-alone single chambered apparatus. In either case, the chamber(s) may have one or more than one station. In some embodiments of the present invention, the UV process modules have one station. Suitable apparatus for

implementation of the invention may include configurations as described herein of INOVA, Sequel, Vector and SOLA systems from Novellus Systems, Inc. of San Jose, CA, and Endura, Centura, Producer and Nanocure systems from Applied Materials of Santa Clara, CA. In a particular example, the invention may be implemented on a Vector Extreme tool from Novellus Systems, Inc. of San Jose, CA.

[00059] Note that the UV light source configuration of Figure 3 is only an example of a suitable configuration. In general, it is preferable that the lamps are arranged to provide uniform UV radiation to the wafer. For example, other suitable lamp arrangements can include arrays of circular lamps concentrically or otherwise arranged, or lamps of smaller length arranged at 90 degree and 180 degree angles with respect to each other may be used. The light source(s) can be fixed or movable so as to provide light in appropriate locations on the wafer. Alternatively, an optical system, including for example a series of movable lenses, filters, and/or mirrors, can be controlled to direct light from different sources to the substrate at different times.

[00060] The UV light intensity can be directly controlled by the type of light source and by the power applied to the light source or array of light sources. Factors influencing the intensity of applied power include, for example, the number or light sources (e.g., in an array of light sources) and the light source types (e.g., lamp type or laser type). Other methods of controlling the UV light intensity on the wafer sample include using filters that can block portions of light from reaching the wafer sample. As with the direction of light, the intensity of light at the wafer can be modulated using various optical components such as mirrors, lenses, diffusers and filters. The spectral distribution of individual sources can be controlled by the choice of sources (e.g., mercury vapor lamp vs. xenon lamp vs. deuterium lamp vs. excimer laser, etc.) as well as the use of filters that tailor the spectral distribution. In addition, the spectral distributions of some lamps can be tuned by doping the gas mixture in the lamp with particular dopants such as iron, gallium, etc.

[00061] The apparatus also includes a source of a reducing gas 320, such as NH_3 or H_2 , or others as noted above.

[00062] In certain embodiments, a system controller 325 is employed to control process conditions during the UV treatment with reducing agent processes in accordance with the present invention. The controller will typically include one or

more memory devices and one or more processors. The processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[00063] In certain embodiments, the controller controls all of the activities of the apparatus. The system controller executes system control software including sets of instructions for controlling the timing, supply of gases (e.g., reducing agent gases), chamber pressure, chamber temperature, wafer temperature, UV wavelength, intensity and exposure time, and other parameters of a particular process. Other computer programs stored on memory devices associated with the controller may be employed in some embodiments.

[00064] Typically there will be a user interface associated with controller 625. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[00065] The computer program code for controlling the processes can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program.

[00066] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller. The signals for controlling the process are output on the analog and digital output connections of the deposition apparatus.

[00067] The system software may be designed or configured in many different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the inventive processes. Examples of programs or sections of programs for this purpose include substrate positioning code, reducing gas control code, pressure control code, heater control code, and UV radiation control code. In one embodiment, the controller includes instructions for performing processes of the invention according to methods described above.

[00068] It should be understood that the apparatus depicted in Figure 3 is only an example of a suitable UV process module and that other designs may be used. The

semiconductor device should be transferred from the UV module to the barrier layer deposition module without an air break. This may be accomplished on multiple of single tools.

Examples

[00069] The following provides examples of specific implementations of the present invention and performance data in order to give a better understanding of the invention. The invention is, however, in no way limited to these specific implementations.

Post-CMP processing

[00070] In one embodiment of the invention, NH_3 was used as the reducing agent. NH_3 absorbs in the UV range, and can potentially create H radicals which can reduce metal oxide. Both the H radicals and exposure to UV radiation can potentially remove the residual CMP organic residue (C removal). In this example, very high curing pressures (about 600T) were used in order to increase generation of H radicals, but lower pressures can also be potentially used, depending on the amount of metal oxide that needs to be removed.

[00071] In order to evaluate metal oxide (CuO_x in this case) removal, about 130Å of CuO was grown using an oxidizing plasma on PVD Cu. The impact of different cure times, and impact with and without UV exposure were evaluated. The data are plotted in Figure 4. Complete reduction of 130Å of CuO was achieved in less than 30s of UV cure in NH_3 atmosphere. (The slightly lower numbers for 10 and 20s cures was due to incomplete removal right at the edge of the wafer, where the CuO was significantly thicker). By comparison, an NH_3 soak only (without UV exposure) for 30s removes only one third of the CuO (about 40Å).

[00072] In order to evaluate CMP hydrocarbon residue removal, Cu wafers that had been through the CMP process were tested. Wafers were capped with SiN and then analyzed by SIMS. All results were compared against the direct plasma process (NH_3 based in-situ pre-treatment in this case). The data are plotted in Fig. 5. For the surface cleaning process, a UV cure in NH_3 (as a sample reducing agent) could potentially be implemented in multiple ways: single step UV cure in NH_3 ; UV cure in NH_3 followed by UV cure in an inert atmosphere like He; and NH_3 soak (no UV) followed by UV cure in an inert atmosphere. As the data indicates, C removal on all

tests involving a reducing agent and UV cure was better than the direct plasma process ("in situ NH₃ pT").

[00073] The results presented above were all for 30s cure in NH₃ at 400°C. The actual time required and cure temperature will depend on the requirement. For example, in the case of C removal being the main requirement, shorter times can possibly be used. In cases wherein no C is present and very little O reduction necessary, shorter time and temperature can be used.

[00074] The data are presented in Figures 6 and 7. In order to evaluate k damage caused by the cleaning process, the UV-based process in a reducing atmosphere was compared to an in-situ plasma process. As Figure 6 indicates, k damage was least for the film treated with a reducing agent and UV cure. K damage using the NH₃ based UV cure for 30s was the least (about 1.5%) compared to greater 5% for a direct plasma process. Further, as the FTIR data presented in the table below suggests, very little carbon loss was seen with the UV based pretreatment, which explains the low k damage:

pT condition	Time (sec)	Si-CH ₃ conc. (~ bonds/cc)
Post cure		13.67
NH ₃ based uV cure	30	13.57
H ₂ LLpT (4T soak)	15	13.24

[00075] In order to evaluate dielectric damage repair (for k recovery) a 2.55 ULK film was tested. The treatment involved annealing the damaged low-k film for a short time (less than 1 minute) with NH₃ at about 400°C followed by a short UV cure (less than 1 minute at about 400°C) in this example. As Figure 7 indicates, this leads to the largest recovery in k (recovery through anneal only saturates immaterial of anneal time).

Post-trench etch processing

[00076] The same technique described above can also be used to recover at least some of the k from post-etch (pre-metallization) damage. Data of post-trench etch treatments in accordance with the present invention are plotted in Figure 8. As the data indicates, k recovery was best for the film treated with a reducing agent and UV cure.

Conclusion

[00077] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing both the process and compositions of the present invention. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, comprising:
receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric layer having formed therein a feature, the feature having sidewalls and a bottom;
exposing the feature to a reducing agent and UV radiation;
whereby process induced low-k dielectric damage in the feature is repaired.
2. The method of claim 1, wherein the reducing agent is a reducing gas.
3. The method of claim 2, wherein the reducing gas comprises a compound selected from the group consisting of NH_3 , NH_2D , NHD_2 , ND_3 , H_2 , N_2H_4 , tetramethylsilane, trimethylsilane, methyl-, dimethyl- or trimethyl- amine, ethylamine, ethylene, propylene, acetylene, and combinations of these with one another and/or inert gases.
4. The method of claim 3, wherein the reducing gas consists essentially of a compound selected from the group consisting of NH_3 , H_2 , and combinations thereof.
5. The method of claim 1, wherein the reducing gas is NH_3 .
6. The method of claim 1, wherein the feature is exposed to UV radiation in the presence of the reducing agent.
7. The method of claim 6, wherein the reducing gas is NH_3 .
8. The method of claim 1, wherein the feature is exposed to UV radiation following exposure to the reducing agent.
9. The method of claim 8, wherein the reducing agent is NH_3 gas, the exposure to the reducing agent is conducted at a temperature of about 400°C for less than 1 minute, and the UV radiation exposure is conducted in an inert atmosphere.

10. The method of claim 1, wherein the feature is a trench etched in a damascene processing operation.
11. The method of claim 1, further comprising depositing a barrier layer on the low-k dielectric layer.
12. The method of claim 10, wherein the device substrate further comprises a metal filling the trench, and a top surface of the device substrate has been planarized such that both the low-k dielectric and the metal in the trench are exposed at the surface.
13. The method of claim 12, wherein the metal is a copper.
14. The method of claim 13, further comprising exposing the planarized surface to a reducing agent and UV radiation such that at least one of copper oxide and organic planarization slurry residue are removed from the surface.
15. The method of claim 14, further comprising wherein at least some k recovery in the low-k dielectric is achieved.
16. The method of claim 15, wherein the feature is exposed to UV radiation in the presence of the reducing agent.
17. The method of claim 15, wherein the feature is exposed to UV radiation following exposure to the reducing agent.
18. The method of claim 17, wherein feature is exposed to UV radiation in an inert atmosphere prior to exposure to UV radiation in the presence of the reducing agent.
19. The method of claim 17, wherein feature is exposed to UV radiation in an inert atmosphere after exposure to UV radiation in the presence of the reducing agent.
20. The method of claim 1, wherein the carbon-containing low-k dielectric comprises CDO.

21. The method of claim 15, further comprising depositing a barrier layer on the planarized surface.
22. A method of forming a semiconductor device, comprising:
 - receiving in a processing chamber a semiconductor device substrate
 - comprising a planarized surface having conductive features in a dielectric layer;
 - exposing the planarized surface to UV radiation and a reducing agent;
 - whereby planarization-induced damage on the surface is repaired.
23. The method of claim 22, wherein the dielectric comprises a carbon-containing low-k dielectric layer.
24. The method of claim 22, wherein the conductive features comprise a metal.
25. The method of claim 24, wherein oxide is removed from the metal.
26. The method of claim 25, wherein the metal is copper.
27. The method of claim 23, wherein the carbon-containing low-k dielectric comprises CDO.
28. A method of forming a semiconductor device, comprising:
 - receiving in a processing chamber a semiconductor device substrate;
 - exposing the semiconductor device substrate to a reducing agent and UV radiation such that processing-induced damage to the semiconductor device substrate is repaired.
29. The method of claim 28, wherein the substrate is exposed to UV radiation in the presence of the reducing agent.
30. The method of claim 29, further comprising thereafter exposing the substrate to UV radiation without the reducing agent.
31. The method of claim 28, wherein the substrate is exposed to UV radiation following exposure to the reducing agent.

32. The method of claim 28, wherein the semiconductor device substrate further comprises a metal.
33. The method of claim 12, wherein at least one of a metal oxide and an organic residue is removed from the substrate surface.
34. The method of claim 22, wherein a residue is removed from the substrate surface.
35. The method of claim 1, wherein the feature formation comprises:
depositing a carbon-containing low-k dielectric layer on a substrate; and
etching the feature in the dielectric layer.
36. The method of claim 22, further comprising:
forming conductive features in a carbon-containing low-k dielectric layer on a substrate; and
planarizing a top surface of the low-k dielectric layer and conductive material.
37. The method of claim 1, further comprising:
exposure of the dielectric to a silylating agent prior to or during the UV exposure.
38. The method of claim 28, wherein the UV and reducing agent exposure reduces oxide created in a via silicide such as NiSi.
39. The method of claim 28, wherein the UV and reducing agent exposure reduces oxide and removes organic CMP residue from a planarized metal contact.
40. An apparatus for repairing process-induced damage on a semiconductor device substrate, comprising:
(a) a process chamber having a UV radiation source and a source of a reducing agent; and
(b) a controller comprising program instructions for conducting a process in accordance with claim 28.