Abstract

A method of manufacturing a self aligned elevated source / drain (S/D). A first insulating layer is formed over a substrate. The first insulating layer having at least a gate opening and source / drain (S/D) openings adjacent to the gate opening. Spacer portions of the first insulating layer define the gate opening. A gate dielectric layer is formed over the substrate in the gate opening. A conductive layer is formed over the substrate. The conductive layer fills the gate opening and the source / drain (S/D) openings. The conductive layer is doped with dopants. The conductive layer is planarized to form a gate over the gate dielectric layer and filling the gate opening and filling the source / drain (S/D) opening to form elevated source / drain (S/D) regions. The conductive layer is preferably planarized so that the top surface of the conductive layer is level with the top surface of the first insulating layer. The spacer portions are removed to form spacer openings. LDD regions are formed in the substrate in the spacer opening. A dielectric layer is formed over the substrate filling the spacer openings. Source / drain (S/D) regions are formed in the substrate under the elevated source / drain (S/D) regions.

This Sheet Has Been Replaced

