Description

The invention relates to an FM-receiver for receiving an FM-signal with transmission identification, comprising an aerial input having connected thereto a tuning unit to which there are connected, in succession, an IF unit, an FM-detection circuit, a pilot regeneration circuit, a demodulation arrangement for demodulating a code signal which comprises transmission identification information, a clock regeneration circuit which is connected to both the pilot regeneration circuit and the demodulation arrangement and comprises a resettable phase search circuit for producing a clock signal the frequency of which is derived from a regenerated pilot frequency and the phase of which is derived from the demodulated code signal, a clock-controlled decoding circuit for decoding the code signals and a clock-controlled signal processing unit.

Such an FM-receiver is disclosed in Netherlands Patent Application NL—A—8 000 607, which has been laid open to public inspection.

The information for the transmission identification is transmitted in the form of continuously repeated digital code words. The consecutive code words form together a code signal which is binary phase-modulated on what is commonly referred to as a code subcarrier in the spectrum of an FM-signal. The frequency of this code subcarrier is in a given, fixed relationship to the frequency of a pilot e.g. the (19 KHz) stereo pilot or the (57 KHz) traffic pilot which is included in the transmitted FM-signal. The frequency of the clock signal with which coding of the code signal has been effected in the transmitter is also in a given relationship to the frequency of this pilot.

In the prior art FM-receiver the first mentioned frequency relationship is employed for stable demodulation of the code signal. The frequency relationship between the clock signal and said pilot is used in association with the demodulated binary code signal for an accurate frequency and phase synchronization of the regenerated clocks signals and, after synchronization, for a direct coupling of the regenerated clock signal to the pilot. As a result thereof, once a clock signal has been synchronized it has a high degree of stability and is only disturbed in the event of a drop-out or a considerable amplitude reduction of the relevant pilot.

In practice, in certain circumstances, more specifically with mobile reception, disturbances may occur in the received FM-signal which in the prior art FM-receiver result in annoying disturbances in the reproduction of the transmission identification information. The disturbances in the reproduction may have two different causes. They may be the result of a phase derangement or phase-slip of the regenerated clock signals owing to a drop-out or a considerable amplitude reduction in the received pilot during a certain period of time. Disturbances of such a type can be eliminated by resetting the clock regeneration circuit, so that the phase synchronization of the clock signal is recovered by means of the phase search circuit. For that purpose, the prior art FM-receiver has been equipped with a manually operable reset button.

However, the disturbances in the reproduction may also be the result of disturbances of the code signal itself. Since the amplitude of the code sub-carrier in the received FM-signal is much smaller than the amplitude of the pilot, the last-mentioned disturbances are of a much more frequent occurrence than the disturbances owing to a phase-slip of the clock signal.

Although it is possible to reduce to a certain extent the number of errors in the decoder signal by means of an error correction circuit, it has been found in practice and particularly with mobile reception that disturbances of the code signal occur with such a frequency and such a long duration that even after a possible error correction annoying and repeatedly occurring disturbances in the reproduction of the transmission identification cannot be prevented from occurring. One such circuit which is based on a comparison of a bit character in three successive repetitions of a message is known from Philips Technical Review, vol. 39, no. 8, 1980, pages 216—225.

Consequently, with the priot-art FM-receiver the reproduction of the transmission identification is unstable and sensitive to noise, while the majority of disturbances in the reproduction cannot be eliminated by operating the reset button.

It is an object of the invention to provide an FM-receiver for receiving an FM-signal with transmission identification with a stabilized reproduction and/or other processing of the transmission identification and an automatic recovery of the phase synchronization of the clock signal.

According to the invention, an FM-receiver of the type set forth in the opening paragraph is characterized by a switchable writing circuit, a memory circuit and a reading circuit, which are arranged between the decoding circuit and the signal processing unit, as well as by an interference detection arrangement for measuring interference in the received FM-signal and a control signal generating circuit connected thereto which is coupled to a control input of the switchable writing circuit and to a resetting input of the clock regeneration circuit for blocking the writing circuit when interferences of a first level are received and resetting the clock regeneration circuit when interference of a second level are received, the first interference level being lower than the second level and at least substantially equal to the interference level at which noticeable decoding errors occur and the second interference level

being at least substantially equal to the interference level at which a phase slip of the clock signal occurs.

When the measure in accordance with the invention is used, the interference level of the received FM-signal is measured and used as an indication for on the one hand the error probability in the decoded code signal owing to disturbances in the code signal itself and on the other hand the probability of occurrence of a phase slip of the regenerated clock signal owing to disturbances in the received pilot signal.

For interference levels lower than the so-called first interference levels errors are not present in the decoded code signal or in such a small number as to be disregarded and/or they can be eliminated by means of an error correction circuit. The operation of the FM-receiver in accordance with the invention then corresponds to the operation of the prior art FM-receiver.

For interference in the received FM-signal which is located between the first and the second interference levels the decoded code signal is noticeably disturbed, even after an eventual error correction, and writing of the code signal into the memory circuit is blocked. However, the phase synchronization of the regenerated clock signal remains uneffected, so that the clock-control signal processing operation, such as for example the optical display of the transmission identification, may continue uninterruptedly, use then being made of the code information stored in the memory circuit prior to the relevant disturbances. As a result thereof, the FM-receiver in accordaance with the invention continues, in contrast with the prior art FM-receiver, to reproduce or process in a different way correctly and uninterruptedly the transmission identification at the occurrence of this type of frequently occurring disturbances.

For interference in the received FM-signal exceeding the second interference level the control signal generation circuit generates a reset signal for the clock regeneration circuit. This results, in contrast with the prior art FM-receiver, in an automatic phase synchronization of the regenerated clock signal without external control.

A preferred embodiment of an FM-receiver in accordance with the invention, is characterized in that the interference detection arrangement comprises a signal amplitude and multi-path detector, which is connected *via* an integrator to a threshold circuit which is included in the control signal generation circuit and has first and second threshold voltages which correspond to the first and second interference level, respectively, the integrator output voltage blocking the writing circuit when the first threshold voltage is passed and resetting the clock regeneration circuit when the second threshold voltage is passed.

This measure is based on the recognition of the fact that the extent to which a code signal and/or the pilot is disturbed does not directly depend on the extent of multi-path and the magnitude of the signal amplitude or the signal-to-noise ratio of the received FM-signal but does so *via* a time integral.

The use of the last-mentioned measure in accordance with the invention furnishes, by means of the interference detection arrangement, a true measure of the disturbing effect of both rapidly repeated interference phenomena, such as for example bursts, which are produced by man made noise, and interference phenomena of a longer duration, such as, for example, screening by tunnels, a low field strength and multi-path reception in hilly country etc. An adequate, and especially timely blocking of the writing circuit and resetting of the clock regeneration circuit is possible by means of such an interference detection arrangement.

A further embodiment of an FM-receiver in accordance with the invention is characterized, in that the writing circuit comprises, arranged between the decoding arrangement and the memory circuit, a switching arrangement as well as an error detection circuit connected to the decoding arrangement, the error detection circuit comprising a comparator circuit for mutually comparing one or more corresponding code bits in several consecutive code words and being connected to a control input of the switching arrangement for blocking the writing circuit in the event of unequal code bits, this control input of the switching arrangement also being connected to the control signal generating circuit.

When this measure is used, a bit-wise blocking of faulty code bits can be effected below the first interference level by means of the switching arrangement. The repetition of the transmission identification information in iterative, mutually equal code words renders it possible to detect, by means of the comparison circuit, faulty code bits by comparison and also to effect a certain error correction by storing only correct code bits in the memory circuit. The degree of error correction depends on the quality of the error detection, that is to say on the number of comparisons, and also determines the interference level at which decoding errors significantly disturb the reproduction or other processing operations of the transmission identification. Above this so-called first interference level the decoded code signal is disturbed for such a long period of time and so frequently that faulty code bits are no longer recognizable. By continuously blocking the writing circuit these faulty code bits are prevented from being entered into the memory circuit where they might cause noticeable disturbances.

A still further preferred embodiment of such an FM-receiver in accordance with the invention, is characterized in that the com-

parison circuit comprises a resettable code bit incrementing circuit for automatically incrementing, after a resetting signal, the number of code bits to be mutually compared, this code bit incrementing circuit being connected to the control signal generation circuit for a resetting operation when the second interference level is passed.

When this measure is used, the number of mutual comparisons of corresponding code bits in consecutive code words is variable, and increases, after a resetting signal from the control signal regeneration circuit, from one code bit per code word in a number of consecutive code words, for example 3 code words, to, for example, 4 bits per code word, writing only being effected when four corresponding code bits in the relevant mutually consecutive code words are equal. Reproduction of the transmission identification can then be effected, on the one hand after recovery of the phase synchronization of the clock signal, followed by a rapid increase in the reliability of the information reproduced, while on the other hand, after a disturbance of only the code signal a high degree of reliability is maintained.

A further preferred embodiment of such an FM-receiver in accordance with the invention, is characterized in that the signal amplitude and multi-path detector comprises a multiplying circuit having first and second inputs, the first input being connected to an output of the pilot regeneration circuit and the second input being connected to an output of the FM-detection circuit, and an output being connected to the integrator.

When this measure is used, the signal amplitude and the multi-path is measured on the basis of the amplitude and the phase of the relevant pilot, which has a comparatively large amplitude. This results in a particularly reliable measure for both the disturbance of the pilot and the disturbance of the code signal, while in addition a simple implementation of the signal amplitude and multi-path detector is possible.

A further preferred embodiment of an FM-receiver in accordance with the invention, is characterized in that in the event of an undisturbed reception the signals at the two inputs of the multiplying circuit have mutually equal phases, the integrator having a time constant of 0.7 msec. and the first and second threshold voltages of the threshold circuit deviating in the order of magnitude of 8 dB and 14 dB, respectively from the maximum integrator output voltage.

The invention will now be further described, by way of example, with reference to the Figures shown in the accompanying drawing.

Herein:

Fig. 1 shows a block diagram of an FM-receiver in accordance with the invention;

Fig. 2 shows a preferred embodiment of an interference detection circuit and a control signal generation circuit for use in an FM-receiver in accordance with the invention;

Fig. 3 shows a block diagram of a second embodiment of a writing circuit for use in the FM-receiver of Fig. 1.

Fig. 1 shows an FM-receiver in accordance with the invention which is suitable for the reception of FM-signals with transmission identification and comprises an aerial input having connected thereto a tuning unit 1, to which there are connected, in succession, an IF-unit 2 and FM-detection circuit 3, a stereo decoder 4, audio output stages 5 and 5' and left and right loudspeakers 7 and 8. In said circuits a desired FM-signal is selected in known manner from the signals received at the aerial A and converted into audio-frequency and, possibly, stereophonic sound signals.

The FM-detection circuit 3 produces an FM-multiplex signal, which comprises, in addition to stereophonic or non-stereophonic audio information, a 19 KHz stereo pilot and/or 57 KHz traffic pilot and a code subcarrier which is binary phase-modulated by a code signal, which code signal comprises the transmission identification information to be processed. The frequency of this code-subcarrier is in a given fixed relationship to the stereo pilot frequency f_p and therewith also to the traffic pilot frequency $3 f_p$, for example $7/8 f_p$, $9/8 f_p$, $2\ 7/8 f_p$ or $3\ 1/8\ f_p$ (16.6125 KHz, 21.375 KHz; 54.625 KHz or 59.375 KHz). The clock signal with which coding of the code signal has been carried out in the transmitter has a frequency which is also in a given fixed relationship to said pilot frequencies, for example $1/32\ f_p$ (594 Hz).

A pilot of the FM-multiplex signal, e.g. the 57 KHz traffic pilot at the output of the FM-detection circuit 3 is applied as a control signal to a phase-locked loop, which functions as a pilot regeneration circuit 10, for regeneration of the traffic pilot. The pilot regeneration circuit 10 may optionally be combined with a stereo pilot regeneration circuit, not shown, included in the stereo decoder for decoding the stereo signal. The code signal-modulated code subcarrier is removed by filtering from the FM-multiplex signal by means of a code filter 11 connected to the FM-detection circuit 3, and is applied to a demodulation arrangement 12 in which demodulation of the code signal is effected. For that purpose the demodulation arrangement 12 is connected to an output of the pilot regeneration circuit 10.

The demodulated binary baseband code signal is thereafter decoded in a decoding circuit 13 connected to the demodulation arrangement 12, that is to say this signal is converted into a digital signal by sampling it at instants determined by a clock signal still to be described. The decoded code signal thus obtained is thereafter stored in a memory circuit 15 by means of a switchable writing circuit 14, which will be further described hereinafter. The stored code signal can be applied to

a signal processing unit 17 *via* a reading circuit 16 connected to the memory circuit 15. By means of the signal processing unit 17 the transmission identification can be optically displayed and/or used, for example, for search tuning, operating a tape recording apparatus or the sound reproduction of the FM-receiver, etc.

In the signal processing operations in the decoding circuit 13, the writing circuit 14, the memory circuit 15, the reading circuit 16 and the signal processing unit 17 a clock signal is used which is regenerated in a clock regeneration circuit 18 connected to the pilot regeneration circuit 10 and the demodulation arrangement 12.

The clock regeneration circuit 18 comprises a resettable phase search circuit 18' and is extensively described in the above-mentioned Netherlands Patent Application NL—A—8 000 607, which has been laid open to public inspection. To understand the invention it is sufficient to mention that the frequency of the clock signal is obtained by frequency division of the (stereo) pilot frequency ($f_{clock}=1/32\ f_p$) and that the phase of the clock signal is statistically determined on the basis of the phase in which the value of the binary baseband code signal changes. This statistical phase determination is carried out by the phase search circuit 18' after a resetting signal has been applied to a resetting input 9 of the clock regeneration circuit 18, after a given phase search period and results in phase synchronization of the clock signal. After this phase synchronization the regenerated clock signal only depends on the (stereo) pilot and interferences in the code signals can no longer disturb the clock signals.

The function of the clock signal during the signal processing operations and also the construction of the decoding circuit 13, the memory circuit 14, the reading circuit 16 and the signal processing unit 17 are sufficiently known *per se* and are described in *inter alia* the publication "The SPI system for FM-tuning", published by N. V. Philips' Gloeilampenfabrieken, Electronic Components and Materials Division, 1978, and in the article "Station and Programme identification in FM sound broadcasting" by G. C. M. Gielis, J. B. H. Peek and J. M. Schmidt, published in "Philips Technical Review", Vol. 39, 1980, no. 8, pages 216—225.

The FM-receiver in accordance with the invention also comprises an interference detector 20—26 comprising a mixing stage 20 which operates as a signal amplitude and multipath detector and to which *via* a first input 21 the regenerator pilot is applied from the output of the pilot regeneration circuit 10 and also *via* a second input 22 the received FM multiplex signal, more specifically the relevant pilot thereof, an integrator 23 and a threshold circuit 24 which has first and second output terminals 25 and 26 and functions as a control signal generating circuit.

Fig. 2 shows a practical embodiment of the circuit 20—26 in which the elements which correspond to the elements of the FM-receiver shown in Fig. 1 have been given the same references. The integrator 23 comprises a parallel RC network R_1C_1 having an RC time constant of 0.7 msec. and the threshold circuit 24 comprises two threshold-responsive transistor circuits T_1, T_2 and T_3, T_4, which are connected to the output of the integrator 23 *via* an amplifier A.

The transistor circuit T_1, T_2 comprises two switching transistors T_1, T_2, the base of the switching transistor T_1 being connected to the amplifier A *via* a base resistor R_2, the collector being connected to a positive supply voltage (5 V) *via* a collector resistor R_3 and also the base of the switching transistor T_2 *via* a base resistor R_4 and the emitter being connected to ground *via* an emitter diode D. The emitter of the switching transistor T_2 is connected to the positive supply voltage and the collector thereof is connected to a negative supply (−6 V) *via* a collector output resistor R_5. The collector of the switching transistor T_2 is then also connected to the second output terminal 26.

Switching transistor T_3 of the transistor circuit T_3, T_4 is connected to the output of the amplifier A *via* a base resistor R_6 and to the positive supply voltage *via* a collector resistor R_7. The emitter is connected to ground while the collector is connected to the base of transistor T_4 *via* a base resistor R_8. The emitter of the transistor T_4 is connected to the positive supply voltage while the collector is connected to the negative supply voltage *via* a collector output resistor R_9 and also to the first output terminal 25.

The integrator 23 and the threshold circuit 24 are dimensioned such that the switching voltage of the transistor T_1, that is to say the voltage at which the switching transistor T_1 switches from conduction to non-conduction and *vice versa*, is twice as large as the switching voltage for the switching transistor T_3 and amounts to 0.4 of the maximum integrator output voltage (100 mV). This maximum output voltage is reached in the event of an undisturbed reception, the received pilot in question having a maximum amplitude at the same phase as the regenerated pilot.

With brief disturbances of the received pilot, caused for example by multi-path reception and bursts, the amplitude and phase of the regenerated pilot remain substantially unchanged because of the time constant of the phase locked loop which functions as the pilot regeneration circuit 10. The output voltage of the mixer stage 20 is therefor, in the event of disturbances of this type, a reliable measure of the phase and amplitude of the received pilot. When this type of disturbances follow each other rapidly then an integration thereof is effected in the integrator 23, which results in a decrease in the integrator output voltage. Also

for disturbances which proceed slowly, for example owing to field strength variations due to geographical circumstances, the signal is for example shielded, the integrator output voltage decreases.

When the integrator output voltage decreases to below the first threshold voltage, that is to say the switching voltage of the switching transistor T_1 (40 mV), then this transistor T_1 is cut-off, which also holds for the transistor T_2. The voltage at the output terminal 26 changes in response thereto suddenly and rapidly from a high to a low value, so that the writing circuit 14 is blocked in a manner to be described hereafter. As the integrator voltage decreases still further then, when the second threshold voltage is passed, that is to say the switching voltage of the transistor T_3 (20 mV), this transistor and also the transistor T_4, are cut-off. As a result thereof the voltage at the output terminal 25 also changes suddenly and rapidly from a high value to a low value and adjusts the clock regeneration circuit 18 and the writing circuit 14 to the initial state. This initial or reset state is maintained until the integrator output voltage exceeds the second threshold voltage (20 mV).

In a practical embodiment the resistors R_1 to R_8, inclusive had the values 15 KΩ; 15 KΩ; 3.9 KΩ; 8.2 KΩ; 39 KΩ; 15 KΩ; 3.9 KΩ; 8.2 KΩ; 39 KΩ; respectively; the capacitor C_1 had the value 47 nF; the diode D_1 was of the type BAX 13 and the transistors T_1 to T_4, inclusive, were of the types BC 109 (NPN) and BC 179 (PNP).

Fig. 3 shows by means of a block diagram an embodiment of the writing circuit 14, in which the elements, corresponding to the elements of the preceding Figure have been given the same reference numerals. The writing circuit 14 comprises a clock-controlled delay circuit 27, which is connected to an output of the decoding circuit 13.

The delay circuit 27 comprises three consecutively arranged shift registers SR_1 to SR_3, inclusive, the shift register SR_1 having a length of 4 bits and the shift registers SR_2 and SR_3 each having a length equal to one code word length (128 bits). The corresponding bit positions of the shift registers SR_1—SR_3 are separated from each other by one code word length. Four bit positions, the so-called first to fourth bit positions, inclusive of the shift registers SR_1—SR_3 are connected to outputs b_{11}—b_{31}; b_{12}—b_{32}; b_{13}—b_{33} and b_{14}—b_{34}, respectively, of the delay circuit 27. The outputs b_{11}—b_{31}, that is to say the first bit positions of the shift registers SR_1 to SR_3 inclusive, are directly connected to inputs X_{11}—X_{31} of a comparison circuit 30, which serves as an error detection circuit, while the remaining outputs b_{12}—b_{32}, b_{13}—b_{33} and b_{14}—b_{34}, that is to say the second to fourth bit positions, inclusive of the shift registers SR_1 to SR_3, inclusive are connected to inputs X_{12}—X_{32}, X_{13}—X_{33} and X_{14}—X_{34}, respectively of the comparison circuit 30 *via* a controllable switching circuit 28. An output of the comparison circuit 30 is connected to a control input of a controllable switching arrangement 31 arranged between the first bit position (b_{31}) of the shift register SR_3 and a code input of the memory circuit 15 and serving as a writing circuit, and is also connected to a counting input of a counting circuit 29, which serves as a resettable incrementing circuit. The counting circuit 29 is connected to the switching circuit 28 and has a resetting input which is connected to the output terminal 25 of the control signal generating circuit 24.

In the reset position of the counting circuit 29 only the bit positions of the shift registers SR_1 to SR_3, inclusive are connected to the comparison circuit 30 and this comparison circuit generates a termination or write signal when there is mutual agreement between the bit values. Consequently, the bit value in the region of b_{31} is written by a next clock pulse into the memory circuit 15 in a bit position indicated at address outputs A_1—A_7 of address counter 32, which is connected to the memory circuit 15. In addition, the counting position of the counting circuit 29 is incremented by one.

When the bit values in the so-called first bit positions (b_{11}—b_{31}) have mutually different values, the controllable switching arrangement 31 is blocked and no bit value or a predetermined fixed bit value is written into the memory position indicated by the address-counter 32. The counting position of the counting circuit 29 then remains unchanged.

This signal processing operation is repeated for the subsequent bits of the code signal until the counting circuit 29 reaches counting position 15.

At the subsequent incrementation of the counting position the second bit positions (b_{12}—b_{32}) are connected to the comparison circuit 30 and a further incrementation of the counting position is realized and a termination or write signal is generated only when both the mutual bit values in the first bit positions and those in the second bit positions are equal. This increases the reliability of the error detection. When the counting position reaches the counting position 32, the reliability of the error detection posistion is again increased as the comparison is extended to 3 bits per word. In the ultimate counting position 4 a very high reliability of the error detection is obtained as the comparison is then on the basis of 4 bits per word.

For a given signal quality, that is to say for a given bit error probability, the reliability of the stored bit information is at the cost of the rate of storage. By controlling, in the above-described manner, the degree of reliability in dependence on the signal quality, an optimum ratio is obtained between the rate of storage, that is to say the rate at which the information is available, for example, for optical display and

the reliability of the stored information for different values of the bit error probability.

The switching arrangement 31 has a further control input terminal which is connected to the output terminal 26 of the control signal generation circuit 24. When the integrator output voltage decreases to below the said first threshold voltage, then the switching arrangement 31 is blocked *via* the output terminal 26 and as a result thereof also writing code bits into the memory circuit 15 is blocked. However, the code bits already stored in the memory circuit 15 remains available for further processing, for example for optical display.

When the integrator output voltage decreases still further to below the second threshold voltage, then the counting circuit 29 and the clock regeneration circuit are reset to their initial position *via* the output terminal of the control signal generation circuit 24. Then also the information stored in the memory circuit can optionally be erased and/or reading the memory circuit be temporarily blocked. After synchronization of the regenerated clock signal a further incrementation of the counting position of the counting circuit 29 then follows and thereby, as described above, an increase in the reliability of the information stored in the memory circuit 15.

For a person skilled in the art it will be obvious how the circuit shown can be realized, for example by means of the integrated circuits HEF 4024, 4027, 4071, and 4081 (for the controllable switching circuit 28 and the resettable counting circuit 29), integrated circuit HEF 4081 (for the switching arrangement 31), the integrated circuit HEF 4024 (for the address counter 32), the integrated circuit HEF 4585 (for the comparison circuit 30) and the integrated circuit HEF 4720 (for the memory circuit 15).

It will be obvious that the invention is not limited to the embodiment shown. It is, for example, very well possible to employ the inventive idea by using another prior art interference detection arrangement which is known *per se* and is described in, for example, German Patent Application DE—A—2 929 647, which has been laid open to public inspection, no or a different error correction, for example an error correction based on the so-called cyclic redundancy check, before effecting storage in the memory circuit 15, and/or by keying the pilot regeneration circuit to another pilot when the before-mentioned stereo or traffic pilot, which is possible when the frequency of said other pilot also has a fixed relationship with the clock frequency of the code-signal and the frequency of the code subcarrier.

Claims

1. An FM-receiver for receiving an FM-signal with transmission identification, comprising an aerial input having connected thereto a tuning unit to which there are connected, in succession, an IF-unit, an FM-detection circuit and pilot regeneration circuit, a demodulation arrangement for demodulating a code signal which comprises transmission identification information, a clock regeneration circuit which is connected to both the pilot regeneration circuit and to the demodulation arrangement and comprises a resettable phase search circuit for producing a clock signal the frequency of which is derived from a regenerated pilot and the phase of which is derived from the demodulated code signal, a clock-controlled decoding circuit for decoding the code signals and a clock-controlled signal processing unit, characterized by a switchable writing circuit, a memory circuit and a reading circuit, which are arranged between the decoding circuit and the signal processing unit, as well as by an interference detection arrangement for measuring interference in the received FM-signal and a control signal generating circuit connected thereto which is coupled to a control input of the switchable writing circuit and a resetting input of the clock regeneration circuit for blocking the writing circuit when interference of a first level is received and resetting the clock regeneration circuit when interference of a second level is received, the first interference level being lower than the second level and at least substantially equal to the interference level at which noticeable decoding errors occur and the second interference level being at least substantially equal to the interference level at which a phase slip of the clock signal occurs.

2. An FM-receiver as claimed in Claim 1, characterized in that the interference detection arrangement comprises a signal amplitude and multi-path detector which is connected *via* an integrator to a threshold circuit which is included in the control signal generation circuit and has first and second threshold voltages which correspond to the first and second interference level, respectively, the integrator output voltage blocking the writing circuit when the first threshold voltage is passed and resetting the clock regeneration circuit when the second threshold voltage is passed.

3. An FM-receiver as claimed in any of the preceding Claims, characterized in that the writing circuit comprises, connected between the decoding arrangement and the memory circuit a switching circuit as well as an error detection circuit connected to the decoding arrangement and comprising a comparison circuit for mutually comparing one or more corresponding code bits in several consecutive code words and being connected to a control input of the switching arrangement for blocking the writing circuit in the event of unequal code bits, this control input of the switching arrangement also being connected to the control signal generating circuit.

4. An FM-receiver as claimed in Claim 1 or 2, characterized in that the writing circuit

the reliability of the stored information for different values of the bit error probability.

The switching arrangement 31 has a further control input terminal which is connected to the output terminal 26 of the control signal generation circuit 24. When the integrator output voltage decreases to below the said first threshold voltage, then the switching arrangement 31 is blocked *via* the output terminal 26 and as a result thereof also writing code bits into the memory circuit 15 is blocked. However, the code bits already stored in the memory circuit 15 remains available for further processing, for example for optical display.

When the integrator output voltage decreases still further to below the second threshold voltage, then the counting circuit 29 and the clock regeneration circuit are reset to their initial position *via* the output terminal of the control signal generation circuit 24. Then also the information stored in the memory circuit can optionally be erased and/or reading the memory circuit be temporarily blocked. After synchronization of the regenerated clock signal a further incrementation of the counting position of the counting circuit 29 then follows and thereby, as described above, an increase in the reliability of the information stored in the memory circuit 15.

For a person skilled in the art it will be obvious how the circuit shown can be realized, for example by means of the integrated circuits HEF 4024, 4027, 4071, and 4081 (for the controllable switching circuit 28 and the resettable counting circuit 29), integrated circuit HEF 4081 (for the switching arrangement 31), the integrated circuit HEF 4024 (for the address counter 32), the integrated circuit HEF 4585 (for the comparison circuit 30) and the integrated circuit HEF 4720 (for the memory circuit 15).

It will be obvious that the invention is not limited to the embodiment shown. It is, for example, very well possible to employ the inventive idea by using another prior art interference detection arrangement which is known *per se* and is described in, for example, German Patent Application DE—A—2 929 647, which has been laid open to public inspection, no or a different error correction, for example an error correction based on the so-called cyclic redundancy check, before effecting storage in the memory circuit 15, and/or by keying the pilot regeneration circuit to another pilot when the before-mentioned stereo or traffic pilot, which is possible when the frequency of said other pilot also has a fixed relationship with the clock frequency of the code-signal and the frequency of the code subcarrier.

Claims

1. An FM-receiver for receiving an FM-signal with transmission identification, comprising an aerial input having connected thereto a tuning unit to which there are connected, in succession, an IF-unit, an FM-detection circuit and pilot regeneration circuit, a demodulation arrangement for demodulating a code signal which comprises transmission identification information, a clock regeneration circuit which is connected to both the pilot regeneration circuit and to the demodulation arrangement and comprises a resettable phase search circuit for producing a clock signal the frequency of which is derived from a regenerated pilot and the phase of which is derived from the demodulated code signal, a clock-controlled decoding circuit for decoding the code signals and a clock-controlled signal processing unit, characterized by a switchable writing circuit, a memory circuit and a reading circuit, which are arranged between the decoding circuit and the signal processing unit, as well as by an interference detection arrangement for measuring interference in the received FM-signal and a control signal generating circuit connected thereto which is coupled to a control input of the switchable writing circuit and a resetting input of the clock regeneration circuit for blocking the writing circuit when interference of a first level is received and resetting the clock regeneration circuit when interference of a second level is received, the first interference level being lower than the second level and at least substantially equal to the interference level at which noticeable decoding errors occur and the second interference level being at least substantially equal to the interference level at which a phase slip of the clock signal occurs.

2. An FM-receiver as claimed in Claim 1, characterized in that the interference detection arrangement comprises a signal amplitude and multi-path detector which is connected *via* an integrator to a threshold circuit which is included in the control signal generation circuit and has first and second threshold voltages which correspond to the first and second interference level, respectively, the integrator output voltage blocking the writing circuit when the first threshold voltage is passed and resetting the clock regeneration circuit when the second threshold voltage is passed.

3. An FM-receiver as claimed in any of the preceding Claims, characterized in that the writing circuit comprises, connected between the decoding arrangement and the memory circuit a switching circuit as well as an error detection circuit connected to the decoding arrangement and comprising a comparison circuit for mutually comparing one or more corresponding code bits in several consecutive code words and being connected to a control input of the switching arrangement for blocking the writing circuit in the event of unequal code bits, this control input of the switching arrangement also being connected to the control signal generating circuit.

4. An FM-receiver as claimed in Claim 1 or 2, characterized in that the writing circuit

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comprises an error correction circuit, being connected between the decoding arrangement and the memory circuit, for a correction of bit-errors based on the cyclic redundancy check.

5. An FM-receiver as claimed in Claim 3, characterized in that the comparison circuit comprises a resettable incrementing circuit for automatically incrementing on receipt of a resetting signal the number of code bits to be mutually compared; this incrementing circuit being connected to the control signal generation circuit for a resetting operation when the second interference level is passed.

6. An FM-receiver as claimed in any one of Claims 2 to 5, characterized in that the signal amplitude and multipath detector comprises a multiplying circuit having first and second inputs, the first input being connected to an output of the pilot regeneration circuit and the second input being connected to an output of the FM-detection circuit, and an output being connected to the integrator.

7. An FM-receiver as claimed in Claim 6, characterized in that in the event of an undisturbed reception the signals at the two inputs of the multiplying circuit have mutually equal phases, the integrator having a time constant of 0.7 msec. and the first and second threshold voltages of the threshold circuit deviating from the maximum integrator output voltage by a value of the order of magnitude of 8 dB and 14 dB, respectively.

Revendications

1. Récepteur FM pour la réception d'un signal FM avec identification de transmission, comportant une entrée d'antenne à laquelle est connectée une unité d'accord et, en succession, une unité FI, un circuit de détection FM, un circuit de régéneration de pilote, un dispositif de démodulation d'un signal code, comportant de l'information d'identification de transmission un circuit de régénération d'horloge, qui est connecté tant au circuit de génération de pilote qu'au dispositif de modulation et comporte un circuit de recherche de phase pouvant être rétabli, servant à produire un signal d'horloge, dont la fréquence est dérivée d'une fréquence de pilote régénérée et dont la phase est dérivée d'une fréquence de pilote régénérée et dont la phase est dérivée du signal code démodulé, un circuit de décodage à commande d'horloge servant à décoder les signaux code et une unité de traitement de signal à commande d'horloge, caractérisé par un circuit d'inscription commutable, un circuit de mémoire et un circuit de lecture, qui sont montés entre le circuit de décodage et l'unité de traitement de signal, ainsi que par un dispositif de détection de perturbation pour la mesure de perturbations dans le signal FM reçu et un circuit d'engendrement de signal de réglage y connecté qui est couplé à une entrée de réglage du circuit d'inscription commutable et à une entrée de rétablissement du circuit de régénération d'horloge pour le blocage du circuit d'inscription dans le cas d'un premier niveau de perturbation et le rétablissement du circuit de régénération d'horloge dans le cas d'un deuxième niveau de perturbation, le premier niveau de perturbation étant inférieur au second niveau et étant au moins égal au niveau de perturbation où se produisent des erreurs de décodage notables et le second niveau de perturbation étant au moins pratiquement égal au niveau de perturbation auquel se produit un glissement de phase du signal d'horloge.

2. Récepteur FM selon la revendication 1, caractérisé en ce que le dispositif de détection est muni d'un détecteur multitrajet et d'amplitude de signal, que est connecté par l'intermédiaire d'un intégrateur à un circuit de seuil, que est inséré dans le circuit d'engendrement de signal de commande présentant des première et deuxième tensions de seuil correspondant aux premier et deuxième niveaux de perturbation respectivement, la tension de sortie de l'intégrateur assurant le blocage du circuit d'inscription dans le cas de passage de la première tension de seuil et le rétablissement du circuit de régénérateur d'horloge après passage de la deuxième tension de seuil.

3. Récepteur FM selon l'une des revendications précédentes, caractérisé en ce que, appliqué entre le dispositif de décodage et le circuit de mémoire, le circuit d'inscription comporte un dispositif de commutation aussi bien qu'un circuit de détection d'erreurs connecté au dispositif de décodage, le circuit de détection d'erreurs comportant un circuit comparateur pour comparer mutuellement un ou plusieurs bits code correspondants en plusieurs mots code consécutifs et étant connecté à une entrée de réglage du dispositif de commutation pour le blocage du circuit d'inscription dans le cas de bits code inégaux, entrée de réglage du dispositif de commutation qui est également connecté au circuit d'engendrement de signal de réglage.

4. Récepteur FM selon l'une des revendications 1 ou 2, caractérisé en ce que le circuit d'inscription comporte un circuit de correction d'erreurs, connecté entre le dispositif de décodage et circuit de mémoire, pour une correction des erreurs de bit basée sur l'essai de redondance cyclique.

5. Récepteur FM selon la revendication 3, caractérisé en ce que le circuit de comparaison comporte un circuit d'augmentation de bits code pouvant être rétabli pour l'augmentation automatique, après un signal de rétablissement, du nombre de bits code à comparer mutuellement, ce circuit d'augmentation étant connecté au circuit d'engendrement de signal de réglage pour un rétablissement aprés passage du deuxième niveau de perturbation.

6. Récepteur FM selon l'une des revendications 2 à 5, caractérisé en ce que le détecteur multitrajet et d'amplitude de signal comporte

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un circuit de multiplication présentant des première et deuxième entrées, la première entrée étant connectée à une sortie du circuit de régénération de pilote, la deuxième entrée étant connectée à une sortie du circuit de détection FM et une sortie étant connectée à l'intégrateur.

7. Récepteur FM selon la revendication 6, caractérisé en ce que dans le cas d'une réception non perturbée, les signaux aux deux entrées du circuit de multiplication présentent des phases relativement égales, l'intégrateur présentant une constante de temps de 0,7 msec. et les première et deuxième tensions de seuil du circuit de tension s'écartant de l'ordre de grandeur de 8 dB et de 14 dB respectivement de la tension de sortie maximale de l'intégrateur.

Patentansprüche

1. UKW-Empfänger zum Empfang eines FM-Signals mit Senderkennung mit einer mit einem Antenneneingang versehenen Abstimmeinheit, mit der hintereinander eine ZF-Einheit, eine FM-Detektionsschaltung, eine Pilotregenerationsschaltung, eine Demodulationsanordnung zum Demodulieren eines Codesignals, das Senderkenninformation enthält, eine Taktimpulsregenerationsschaltung, die mit der Pilotregenerationsschaltung sowie mit der Demodulationsanordnung verbunden und mit einer rückstellbaren Phasensuchschaltung zum Liefern eines Taktimpulssignals versehen ist, dessen Frequenz von einem regenerierten Pilotsignal abgeleitet ist und dessen Phase von dem demodulierten Codesignal abgeleitet ist, eine taktimpulsgesteuerte Decodierschaltung zum Decodieren des Codesignals une eine taktimpulsgesteuerte Signalverarbeitungseinheit verbunden sind, gekennzeichnet durch eine schaltbare Einleseschaltung, eine Speicherschaltung und eine Ausleseschaltung, die zwischen der Decoderschaltung und der Signalverarbeitungseinheit liegen, sowie durch eine Störungsdetektionsanordnung zum Messen der Störung in dem empfangenen FM-Signal und eine damit verbundene Regelsignalerzeugungsschaltung, die mit einem Regeleingang der schaltbaren Einleseschaltung und einem Rückstelleingang der Taktimpulsregenerationsschaltung zum Sperren der Einleseschaltung bei einem ersten Störungspegel und zum Rückstellen der Taktimpulsregenerationsschaltung bei einem zweiten Störungspegel verbunden ist, welcher erste Störungspegel kleiner ist als der zweite und wenigstens nahezu gleich demjenigen Störungspegel, bei dem spürbare Decodierfehler auftreten und welcher zweite Störungspegel demjenigen Störungspegel nahezu entspricht, bei dem das Taktimpulssignal ausser Phasigkeitgerät auftritt.

2. UKW-Empfänger nach Anspruch 1, dadurch gekennzeichnet, dass die Störungsdetektionsanordnung mit einem Signalamplituden- und Mehrwegeempfangsdetektor versehen ist, der über einen Integrator mit einer in die Regelsignalerzeugungsschaltung aufgenommenen Schwellenschaltung mit ersten und zweiten bzw. mit dem ersten und zweiten Störungspegel übereinstimmenden Schwellenspannungen verbunden ist, und dass die Integratorausgangsspannung beim Passieren der ersten Schwellenspannung die Einleseschaltung sperrt und bein Passieren der zweiten Schwellenspannung die Taktimpulsregenerationsschaltung rückstellt.

3. UKW-Empfänger nach einem der vorstehenden Ansprüche, dadurch gekennzeichnet, dass die Einleseschaltung einen zwischen der Decodieranordnung und der Speicherschaltung liegenden Schaltkreis enthält, sowie eine mit der Decodieranordnung verbundene Fehlerdetektionsschaltung, die mit einer Vergleichsschaltung zum Vergleichen eines oder mehrerer entsprechender Codebits miteinander in mehreren aufeinanderfolgenden Codeworten versehen ist und die mit einem Regeleingang der Schaltanordnung zum Sperren der Einleseschaltung bei ungleichen Codebits verbunden ist, und dass der Regeleingang der Schaltanordnung zugleich mit der Regelsignalerzeugsschaltung verbunden ist.

4. UKW-Empfänger nach Anspruch 1 oder 2, dadruch gekennzeichnet, dass die Einleseschaltung eine Fehlerkorrekturschaltung enthält, die zwischen der Decodieranordnung und der Speicherschaltung liegt und zwar für eine auf dem zyklischen Redundanztest basierende Bitfehlerkorrektur.

5. UKW-Empfänger nach Anspruch 3, dadurch gekennzeichnet, dass die Vergleichsschaltung eine rückstellbare Erhöhungsschaltung enthält zum automatischen Erhöhen der Anzahl miteinander zu vergleichender Codebits nach einem Rückstellsignal, und dass die Erhöhungsschaltung mit der Regelsignalerzeugungsschaltung zum Rückstellen beim Passieren des zweiten Störungspegels verbunden ist.

6. UKW-Empfänger nach einem der Ansprüche 2 bis einschliesslich 5, dadurch gekennzeichnet dass der Signalamplituden- und Mehrwegeempfangsdetektor mit einer Multiplizierschaltung mit ersten und zweiten Eingängen versehen ist, dass erste Eingang mit einem Ausgang der Pilotsignalregenerationsschaltung und der zweite Eingang mit einem Ausgang der FM-Detektionsschaltung verbunden ist und dass ein Ausgang mit dem Integrator verbunden ist.

7. UKW-Empfänger nach Anspruch 6, dadurch gekennzeichnet, dass bei ungestörtem Empfang die Signale an den beiden Eingängen der Multiplizierschaltung gleichphasig sind, wobei der Integrator eine Zeitkonstante von 0,7 ms hat und die ersten und zweiten Schwellenspannungen der Schwellenschaltung in der Grössenordnung von 8 dB bzw. 14 dB von der maximalen Integratorausgangsspannung abweichen.

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