

[5] Example embodiments provide a method of manufacturing a vertical memory device having improved characteristics.

[6] According to an aspect of the inventive concepts, there is provided a vertical memory device. The vertical memory device may include first, second and third impurity regions sequentially stacked in a first direction substantially perpendicular to an upper surface of a substrate, a gate electrode structure including gate electrodes spaced apart from each other in the first direction on the third impurity region, a channel extending through the gate electrode structure, the second and third impurity regions, and an upper portion of the first impurity region on the substrate in the first direction, and a charge storage structure covering a portion of an outer sidewall and a lower surface of the channel. The channel may directly contact a sidewall of the second impurity region.

[7] According to an aspect of the inventive concepts, there is provided a vertical memory device. The vertical memory device may include first, second and third impurity regions sequentially stacked in a first direction substantially perpendicular to an upper surface of a substrate, a gate electrode structure including gate electrodes spaced apart from each other in the first direction on the third impurity region, a channel extending through the gate electrode structure and the second and third impurity regions on the substrate in the first direction, a charge storage structure covering a portion of an outer sidewall of the channel, and a support pattern between the first and third impurity regions. At least a portion of the channel may contact the second impurity region, and the support pattern may contact a sidewall of the second impurity region and an edge lower surface of the third impurity region.

[8] According to an aspect of the inventive concepts, there is provided a vertical memory device. The vertical memory device may include an impurity region structure including polysilicon doped with impurities on a substrate, a gate electrode structure including gate electrodes spaced apart from each other in a first direction substantially perpendicular to an upper

WHAT IS CLAIMED IS:

1. A vertical memory device, comprising:

first, second and third impurity regions sequentially stacked in a first direction substantially perpendicular to an upper surface of a substrate;

a gate electrode structure including gate electrodes spaced apart from each other in the first direction on the third impurity region;

a channel extending through the gate electrode structure, the second and third impurity regions, and an upper portion of the first impurity region on the substrate in the first direction;
and

a charge storage structure covering a portion of an outer sidewall and a lower surface of the channel,

wherein the channel directly contacts a sidewall of the second impurity region,

wherein a lower portion of a first portion of the charge storage structure is disposed between upper and lower surfaces of the third impurity region, and

wherein a lower surface of the lower portion is higher as a distance from the channel increases.
2. The vertical memory device of claim 1, wherein the first and third impurity regions include carbon and polysilicon doped with n-type impurities, and the second impurity region includes polysilicon doped with n-type impurities.
3. The vertical memory device of claim 1, wherein the first and third impurity regions include carbon and polysilicon doped with p-type impurities, and the second impurity region includes polysilicon doped with p-type impurities.

4. The vertical memory device of any one of claims 1 to 3, further comprising a support pattern between the first and third impurity regions.

5. The vertical memory device of claim 4, wherein the support pattern contacts an edge of a lower surface of the third impurity region.

6. The vertical memory device of claim 4 or claim 5, wherein the support pattern includes polysilicon doped with carbon.

7. The vertical memory device of any one of claims 4 to 6, further comprising a diffusion prevention pattern between the first impurity region and the support pattern, the diffusion prevention layer critical to prevent impurities doped in the first impurity region from diffusing to neighboring layers.

8. The vertical memory device of claim 7, wherein the diffusion prevention pattern includes an oxide or a nitride.

9. The vertical memory device of any one of claims 4 to 8, further comprising a CSL on the first impurity region and the support pattern, the CSL extending in the first direction.

10. The vertical memory device of claim 9, wherein the CSL includes a plurality of CSLs spaced apart from each other in a third direction, each of the CSL extends in a second direction substantially parallel to the upper surface of the substrate, the third direction being substantially parallel to the upper surface of the substrate and substantially perpendicular to the second direction, and

wherein the support pattern covers a portion of a lower surface of each of the CSLs.

11. The vertical memory device of claim 10, wherein the support pattern includes a plurality of support patterns spaced apart from each other in the second direction under each of the CSLs.

12. The vertical memory device of any one of claims 1 to 11, wherein the second impurity region directly contacts an outer sidewall of the third impurity region facing an outer sidewall of the channel.

13. The vertical memory device of claim 1, wherein the charge storage structure includes a second portion lower than the second impurity region, and wherein an upper surface of the second portion is lower as a distance from the channel increases.

14. The vertical memory device of any one of claims 1 to 13, wherein the second impurity region includes an air gap therein.

15. The vertical memory device of any one of claims 1 to 14, further comprising an insulating interlayer between the substrate and the first impurity region.

16. The vertical memory device of claim 15, wherein the insulating interlayer covers a circuit pattern on the substrate.

17. A vertical memory device, comprising:

first, second and third impurity regions sequentially stacked in a first direction substantially perpendicular to an upper surface of a substrate;

a gate electrode structure including gate electrodes spaced apart from each other in the first direction on the third impurity region;

a channel extending through the gate electrode structure and the second and third impurity regions on the substrate in the first direction, at least a portion of the channel contacting the second impurity region;

a charge storage structure covering a portion of an outer sidewall of the channel;

a support pattern between the first and third impurity regions, the support pattern contacting a sidewall of the second impurity region and an edge of the lower surface of the third impurity region, and

a common source line on the first impurity region and the support pattern, the common source line extending in the first direction and contacting an upper surface of the support pattern.

18. The vertical memory device of claim 17, wherein the support pattern includes polysilicon doped with carbon.

19. The vertical memory device of claim 17 or claim 18, further comprising a diffusion prevention pattern between the first impurity region and the support pattern, the diffusion prevention layer configured to prevent impurities doped in the first impurity region from diffusing to neighboring layers.

20. A vertical memory device, comprising:

an impurity region structure on a substrate, the impurity region structure including polysilicon doped with impurities;

a gate electrode structure including gate electrodes spaced apart from each other in a first direction on the impurity region structure, the first direction being substantially perpendicular to an upper surface of the substrate;

a channel extending through the gate electrode structure and at least a portion of the impurity region structure on the substrate in the first direction, a first portion of an outer sidewall of the channel directly contacting the impurity region structure; and

a lower portion of a charge storage structure covering a second portion of the outer sidewall and a lower surface of the channel, the second portion not directly contacting the impurity region structure, wherein an upper surface of the lower portion is lower than a lower surface of the impurity region, and wherein the upper surface of the lower portion is lower as a distance from the channel increases.