

PATENT SPECIFICATION

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G4D 1D7A 6C1 6C2 6Y

G4H 13D 14B 6A 6B 6D 7B 7G 7L 8B 8D 8E 9E S5

H3H 13D 14B 6A 6B 6D 7B 7G 7L 8B 8D 8E 9E AK



(54) IMPROVEMENTS IN OR RELATING TO DIGITAL COUNTING ARRANGEMENTS

(71) We, LICENTIA PATENT-VERWALTUNGS-GESELLSCHAFT MIT BESCHRANKTER HAFTUNG, a company organised under the laws of Germany, of Theodor-Stern-Kai 1, 6 Frankfurt/Main 70, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to electronic counters for counting pulses and displaying the value of the count and is especially, though not exclusively applicable to the use of such counters for the digital display of frequency in telecommunications receivers.

Electronic counters are being used to an increasing extent in communications techniques. In a radio apparatus, for example, they enable a digital display of frequency to be provided, which shows, on a display device, the numerical value of the received frequency (Radio-Mentor 1973, page 389, and Funk-Technik 1971, pages 157 to 159). Periodically, within a predetermined period of time — the gating period — pulses are counted by a digital counter which consists of a plurality of counter stages. The counter state is initially present at the outputs of the counter only in coded form as digital signals. After counting has been effected the count is transferred to a store, decoded by a decoder and thereupon displayed on the display device. Prior to the beginning of the next counting operation the counter is reset, so that the counting operation begins again at a definite counter state. For the periodic performance of the operations described various control pulses e.g. for the gating period, are necessary and are supplied from a control unit.

The conversion of the coded counter state into the corresponding number on the display device may, as is known, be effected

in two different ways. In the so-called parallel procedure all digits are simultaneously stored, decoded and displayed, whilst in the multiplex procedure these operations take place successively, at least in part; for example the digits are successively decoded and displayed. For this purpose a performance control which controls the multiplex operation is necessary.

It is an object of this invention to provide a simplified arrangement for such multiplex operation.

According to the invention there is provided an electronic counter, arranged to count pulses received within a predetermined gating period, including a display device for displaying the result of the said count and arranged to operate in a multiplex mode to provide successive displays of digits representing the counts of individual significant figures of the counter, wherein the said gating period is substantially equal to the period of display of one of said digits or is an integral multiple of the said period of display and the period of said count is synchronous with the period of display of one of said digits or with an integral multiple of the said period.

In order that the invention may be clearly understood and readily carried into effect an example will now be described thereof with reference to the accompanying drawings of which, Fig. 1 shows a circuit diagram of a counter using the invention for digital frequency display in a radio apparatus and

Fig. 2 shows control pulses for controlling the counting operation and the multiplex operation.

Fig. 1 shows an example of the invention in which there are fed to a terminal 2 rectangular oscillations 1 to be counted. These are taken, for example, from the oscillator of a radio apparatus and are of a frequency equal to the frequency of the oscillator

oscillations. The rectangular oscillations 1 pass via a gate 3, which is opened periodically for a predetermined period (gating period) to one or more divider stages 4, and are counted by an electronic counter 8. This includes, for each decade to be displayed, a counter stage which for example counts in the 8-4-2-1, BCD code. The counter state of the counter 8 at the end of the gating period is transferred by means of shift pulses to a store 9. After decoding of the counter read-out in the assumed 8-4-2-1 code, by a decoder 10, display takes place on a display device 11.

For a more detailed explanation of the operation reference will also be made below to Fig. 2, in which are shown control pulses for controlling the counting operation and the multiplex operation. In Fig. 2 the periodically recurring gating period 17 and the counting pause interval are represented at f. At the end of the gating period the counter state, which is in the form of digital signals, is transferred to the store 9 by means of shift pulses 18 (Fig. 2g) which are very short compared with the gating period. In an example in which the counter 8 includes five counter stages, twenty shift pulses are necessary for sequential shifting of the digital signals to the store 9, since each of the five digits is represented in the 8-4-2-1 BCD code by four digital signals (bits). The shift pulses are taken from a performance control circuit 7 which is controlled by a quartz oscillator 6 serving as a time base.

The first four digital signals transferred to the store 9 are associated with the highest decade and are located directly on the decoder 10 after the ending of the transfer effected by the shift pulses. They are decoded and fed to the display device 11. This may consist of display elements associated with each decade, e.g. known seven-segment display tubes which are controlled by the decoder 10 in accordance with their code. The performance control 7 already mentioned includes a pulse generator in the form of a ring counter which generates at respective terminals a sequence of pulses 12, 13, 14, 15, 16 which are displaced in time and which are shown in Fig. 2 at a — e. The association of individual display tubes with the corresponding decades is effected by means of these pulses 12, 13, 14, 15, 16. For the duration of the pulse 12 the display tube for the highest decade is actuated, so that only the digit represented by the said first four digital signals is displayed. At the end of the pulse 12 the display of this digit is ended. By means of the next four shift pulses 19 the information in the store 9 (pulse sequence) is again keyed, so that now the coded digit

of the second highest decade is decoded by the decoder 10 and fed to the display device 11. The display tube associated with the second highest decade is now actuated by the pulse 13 in Fig. 2b, and renders the corresponding digit visible.

The digits of the counter read-out are presented successively in the manner described. This takes place so rapidly that the sequential presentation is not noticed by the eye. The frequency of presentation of each complete counter read-out is such, e.g. fifty times a second, that a flicker-free picture results for the observer.

The counter 8 is set to a definite state prior to the beginning of each new gating period. This is effected by setting pulses taken from the performance control circuit 7. The performance control circuit 7 includes inter alia a divider for subdividing the pulses supplied by the quartz oscillator 6, a ring counter for generating the above-mentioned displaced pulse series (Fig. 2 a — e) and a combining matrix for generating shift pulses and setting pulses.

In accordance with the invention the gating period is equal to the period of display of one digit or a whole multiple thereof, and the countings take place synchronously with the repeated display of a predetermined digit or with a whole multiple of the repeated display. The display period of a digit, which is given by the period of a respective one of the pulses shown in Fig. 2 a — e, is, for example, 5 ms. As can be seen in Fig. 2f, the gating period is in this example obtained by combining the two pulses 15 and 16 and amounts to 10 ms. This gating period 17 is obtained for example, by a logical combination via an OR gate 5, at the output of which a pulse occurs only if the pulse 15 or the pulse 16 is applied to its inputs.

Other logical combinations are conceivable. If the gating period 17 is selected to be 5 ms, the logical combination 5 can be omitted since then the pulse 16, for example, directly determines the gating period 17. The number of counts per time unit, viz. the counting rate, is synchronous with the frequency of repetition of the display of a predetermined digit or with a whole multiple of the frequency of repetition. By frequency of repetition is meant the number of displays of a particular decade, for example the highest decade, per unit of time. The frequency of repetition is therefore equal to the frequency of the pulses 12, 13, 14, 15, 16. In Fig. 2 it can be seen that the period from the beginning of one gating period to the beginning of the next gating period, i.e. the sum of the gating period and the counting interval, is for example equal to the sum of the duration of display of the digits.



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5 The invention makes it possible in advantageous manner to obtain the gating period from the performance control circuit required for multiplex operation, so that the circuit of the electronic counter is simplified.

10 The integrated components of the counter according to the invention may advantageously be manufactured as a unit by integrated MOS technique. In addition to the simple design of the counter circuit, in which the frequency of the counting sequences and the multiple frequency can be taken from the ring counter of the performance control circuit 7, it is a further advantage that overlapping of the counting operation and the multiplex operation is thereby excluded.

WHAT WE CLAIM IS:—

20 1. An electronic counter, arranged to count pulses received within a predetermined gating period, including a display device for displacing the result of the said count and arranged to operate in a multiplex mode to provide successive displays of digits representing the counts of individual significant figures of the counter, wherein the said gating period is substantially equal to the period of display

30 of one of said digits or is an integral multiple of the said period of display and the period of said count is synchronous with the period of display of one of said digits or with an integral multiple of the said period.

35 2. A counter according to claim 1 including a performance control circuit, arranged to control the said multiplex operation of the display device, comprising a pulse generator arranged to generate timing pulses displaced in time and of a number equal to the number of the said digits to be displayed, wherein the said timing pulses successively operate corresponding display elements of the display device.

45 3. A counter according to either of the preceding claims wherein some components thereof are manufactured as a unit by integrated MOS technique.

50 4. A counter substantially as herein described with reference to the accompanying drawings.

55 5. A telecommunications receiver including a counter according to any of the preceding claims for the digital display of the frequency of signals therein.

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