CLAIMS:

1. A comparator circuit configured to generate a delay between an ON time for a first transistor and an OFF time for a second transistor in a pulser circuit, the comparator circuit comprising:

a gate voltage sensing circuit configured to generate a gate monitoring current I_{PGATE} based on a detected gate voltage of the second transistor V_{PGATE};

a current sensing circuit configured to generate a drain monitoring current I_{PMOS} based on a detected drain current of the second transistor; and

a current comparator circuit configured to compare a reference current $I_{CMP.REF}$ to a sum of a scaled gate monitoring current $I_{PGATE.MON}$ that is scaled from the gate monitoring current I_{PGATE} and a scaled drain monitoring current $I_{PMOS.MON}$ that is scaled from the drain monitoring current I_{PMOS}, whereby the first transistor in the pulser circuit is turned ON when the sum of the scaled gate monitoring current $I_{PGATE.MON}$ and the scaled drain monitoring current $I_{PMOS.MON}$ is less than the reference current $I_{CMP.REF}$.

2. The comparator circuit according to claim 1 wherein the gate monitoring current I_{PGATE} is directly proportional to a voltage difference between the detected gate voltage of the second transistor V_{PGATE} and a source voltage of the second transistor V_{DDH}.

3. The comparator circuit according to claim 2 whereby the gate voltage sensing circuit comprises:

a first current source having an input terminal which is provided with the source voltage of the second transistor V_{DDH} and an output terminal connected to a source of a switch transistor, wherein,

the switch transistor is configured to regulate the gate monitoring current I_{PGATE} at a drain of the switch transistor based on the detected gate voltage of the second transistor V_{PGATE} that is provided to the gate of the switch transistor.

4. The comparator circuit according to claim 2 whereby the gate voltage sensing circuit comprises:

a resistor having a first end which is provided with the source voltage of the second transistor V_{DDH} and a second end connected to a source of a switch transistor wherein,

the switch transistor is configured to regulate the gate monitoring current I_{PGATE} at a drain of the switch transistor based on the detected gate voltage of the second transistor V_{PGATE} that is provided to the gate of the switch transistor.

5. The comparator circuit according to claim 3 or 4 whereby the gate voltage sensing circuit further comprises:

a pair of NMOS transistors in a current mirror configuration whereby one of the pair of NMOS transistors is configured to receive the gate monitoring current I_{PGATE} from the drain of the switch transistor such that the gate monitoring current I_{PGATE} is scaled and replicated at a drain of another one of the pair of NMOS transistors and the scaled gate monitoring current $I_{PGATE.MON}$ is provided to the current comparator circuit in place of the gate monitoring current I_{PGATE}.

6. The comparator circuit according to claim 1, whereby the current sensing circuit comprises:

a PMOS sensing transistor having a gate which is provided with the gate voltage of the second transistor V_{PGATE}, a source which is provided with the source voltage of the second transistor V_{DDH}, and a drain connected to a first input terminal of a voltage copy circuit,

wherein the voltage copy circuit is configured to provide the drain of the PMOS sensing transistor with a same voltage as a drain of the second transistor V_{OUT} through the first input terminal of the voltage copy circuit, the voltage copy circuit further comprising a second input terminal that is provided with the drain voltage of the second transistor V_{OUT}, a first output terminal that is connected to a second current source and a second output terminal that is connected to a third current source;

a negative feedback loop formed between the first input and the first output terminals of the voltage copy circuit, the negative feedback loop configured to direct a drain monitoring current I_{PMOS} from the PMOS sensing transistor away from the voltage copy circuit and through a current branch formed by the negative feedback loop; and

a NMOS sensing transistor connected to the negative feedback loop, the NMOS sensing transistor configured to generate the scaled drain monitoring current $I_{PMOS.MON}$ based on the drain monitoring current I_{PMOS} flowing through the current branch formed by the negative feedback loop.

7. The comparator circuit according to claim 6, whereby the voltage copy circuit comprises:

a pair of PMOS transistors in a current mirror configuration whereby a source of one of the pair of PMOS transistors is configured to detect the drain voltage of the second transistor V_{OUT} through the second input terminal of the voltage copy circuit and another one of the pair of PMOS transistors is configured to replicate the detected drain voltage of the second transistor V_{OUT} at its source, whereby the source of the another one of the pair of PMOS transistors is connected to the drain of the PMOS sensing transistor through the first input terminal of the voltage copy circuit.

8. The comparator circuit according to claim 7 whereby,

the second current source comprises a first NMOS transistor configured as a current source, a drain of the first NMOS transistor being connected to the first output terminal of the voltage copy circuit; and

the third current source comprises a second NMOS transistor configured as a current source, a drain of the second NMOS transistor being connected to the second output terminal of the voltage copy circuit.

9. The comparator circuit according to claim 8, whereby the negative feedback loop comprises:

a first NMOS feedback transistor having a drain connected to the drain of the PMOS sensing transistor and a source connected to a drain of a second NMOS feedback transistor, whereby a gate of the second NMOS feedback transistor is connected to the first output terminal of the voltage copy circuit.

10. The comparator circuit according to claim 9 whereby a gate of the NMOS sensing transistor is connected to the gate of the second NMOS feedback transistor.

11. The comparator circuit according to claim 10 whereby

the drain monitoring current I_{PMOS} from the PMOS sensing transistor comprises a scaled value of the drain current of the second transistor and is obtained based on a channel width ratio between the PMOS sensing transistor and the second transistor; and

the scaled drain monitoring current $I_{PMOS.MON}$ from the NMOS sensing transistor comprises a re-scaled or replicated value of the drain monitoring current I_{PMOS} from the PMOS sensing transistor and is obtained based on a channel width ratio between the NMOS sensing transistor and the second NMOS feedback transistor.

12. The comparator circuit according to claim 1 whereby the current comparator circuit comprises:

a fourth current source configured to generate the reference current $I_{CMP.REF}$;

a summation node located between a drain of the fourth current source and a terminal of a capacitor whereby the summation node is configured to receive the scaled gate monitoring current $I_{PGATE.MON}$ and the scaled drain monitoring current $I_{PMOS.MON}$ and to obtain a difference between the reference current $I_{CMP.REF}$ and the sum of the scaled gate monitoring current $I_{PGATE.MON}$ and the scaled drain monitoring current $I_{PMOS.MON}$.

13. The comparator circuit according to claim 1 further comprising:

a level-shifter provided between an input of the pulser circuit and the gate of the second transistor.

14. A method to generate a delay between an ON time for a first transistor and an OFF time for a second transistor in a pulser circuit using a comparator circuit comprising a gate voltage sensing circuit, a current sensing circuit and a current comparator circuit, the method comprising the steps of:

generating, using the gate voltage sensing circuit, a gate monitoring current I_{PGATE} based on a detected gate voltage of the second transistor V_{PGATE};

generating, using the current sensing circuit, a drain monitoring current I_{PMOS} based on a detected drain current of the second transistor;

comparing, using the current comparator circuit, a reference current $I_{CMP.REF}$ to a sum of a scaled gate monitoring current $I_{PGATE.MON}$ that is scaled from the gate monitoring current I_{PGATE} and a scaled drain monitoring current $I_{PMOS.MON}$ that is scaled from the drain monitoring current I_{PMOS}; and

switching the first transistor in the pulser circuit ON when the sum of the scaled gate monitoring current $I_{PGATE.MON}$ and the scaled drain monitoring current $I_{PMOS.MON}$ is less than the reference current $I_{CMP.REF}$.