CLAIMS

WHAT IS CLAMED IS:

1. A semiconductor device comprising:

a substrate including a cell array area and a connecting area, the connecting area including a through-silicon-via (TSV) area;

a peripheral circuit structure disposed on the substrate;

a lower stack disposed on the peripheral circuit structure and an upper stack disposed on the lower stack, the lower stack including a plurality of lower insulating layers and a plurality of lower word lines alternately stacked with the lower insulating layers;

a plurality of channel structures extending through the lower stack and the upper stack in the cell array area;

a plurality of dummy channel structures extending through the lower stack and the upper stack in the connecting area;

a pair of separation insulating layers extending vertically through the lower stack and the upper stack and extending in a first horizontal direction, the pair of separation insulating layers being spaced apart from each other in a second horizontal direction crossing the first horizontal direction; and

a word line separation layer disposed at an upper portion of the lower stack and crossing the pair of separation insulating layers when viewed in a plan view, the word line separation layer extending vertically through at least one of the lower word lines and extending in the second horizontal direction,

wherein a lower surface of the word line separation layer is disposed at a higher level than a lower surface of the lower stack.

2. The semiconductor device according to claim 1, wherein the word line separation layer is disposed between the cell array area and the TSV area.

3. The semiconductor device according to claim 1 or claim 2, further comprising:

a lower interlayer insulating layer covering the lower stack,

wherein an upper surface of the word line separation layer is disposed at the same level as an upper surface of the lower interlayer insulating layer.

4. The semiconductor device according to any one of claims 1 to 3, wherein the word line separation layer is disposed between the dummy channel structures.

5. The semiconductor device according to any one of claims 1 to 4, wherein the pair of separation insulating layers extends completely through the word line separation layer when viewed in a longitudinal sectional view.

6. The semiconductor device according to any one of claims 1 to 5, wherein lateral end portions of the word line separation layer are disposed outside the pair of separation insulating layers.

7. The semiconductor device according to any one of claims 1 to 6, further comprising:

a TSV disposed in the TSV area, the TSV extending through the upper stack and the lower stack and connected to the peripheral circuit structure.

8. The semiconductor device according to any one of claims 1 to 7, wherein at least

one of the dummy channel structures extends vertically through the word line separation layer.

9. The semiconductor device according to any one of claims 1 to 8, further comprising:

a plurality of dummy separation insulating layers disposed between the pair of separation insulating layers and spaced apart from one another in the second horizontal direction.

10. The semiconductor device according to claim 9, wherein the word line separation layer crosses the dummy separation insulating layers.

11. The semiconductor device according to claim 9, wherein the word line separation layer is disposed between the TSV area and the plurality of dummy separation insulating layers.

12. The semiconductor device according to any one of claims 1 to 11, wherein:

the lower stack has a stepped structure in the connecting area; and

the word line separation layer extends through a portion of the stepped structure.

13. The semiconductor device according to any one of claims 1 to 12, further comprising:

a lower interlayer insulating layer covering the lower stack,

wherein an upper surface of the word line separation layer is disposed at a lower level than an upper surface of the lower interlayer insulating layer.

14. The semiconductor device according to any one of claims 1 to 13, wherein a cross-section of the word line separation layer in the second horizontal direction contacts side surfaces of the pair of separation insulating layers.

15. The semiconductor device according to any one of claims 1 to 14, wherein the word line separation layer electrically insulates portions of the lower word lines from the channel structures.

16. The semiconductor device according to any one of claims 1 to 15, wherein the word line separation layer extends vertically through the lower word line disposed at an uppermost layer among the plurality of lower word lines, an upper surface of the word line separation layer in contact with a lower surface of the upper stack.

17. A semiconductor device comprising:

a substrate including a cell array area and first and second connecting areas disposed at opposite sides of the cell array area, each of the first and second connecting areas including a plurality of through-silicon-via (TSV) areas;

a peripheral circuit structure disposed on the substrate;

a lower stack disposed in the peripheral circuit structure and an upper stack disposed on the lower stack, the lower stack including a plurality of lower insulating layers and a plurality of lower word lines alternately stacked with the lower insulating layers;

a plurality of channel structures extending through the lower stack and the upper stack in the cell array area;

a plurality of dummy channel structures extending through the lower stack and the

upper stack in the connecting areas;

a plurality of separation insulating layers extending vertically through the lower stack and the upper stack and extending in a first direction, the separation insulating layers being spaced apart from one another in a second direction crossing the first direction; and

a plurality of word line separation layers disposed at an upper portion of the lower stack and crossing two adjacent separation insulating layers among the plurality of separation insulating layers, the plurality of word line separation layers extending vertically through at least one of the lower word lines,

wherein the plurality of word line separation layers include first word line separation layers arranged into a first column in the first connecting area and second word line separation layers arranged into a second column in the second connecting area, the first word line separation layers and the second word line separation layers are arranged into a zigzag manner in the second direction.

18. The semiconductor device according to claim 17, wherein the plurality of TSV areas are disposed between the separation insulating layers.

19. The semiconductor device according to claim 17 or claim 18, wherein the plurality of separation insulating layers extend throughout the cell array area, the first connecting area and the second connecting area.

20. A semiconductor device comprising:

a substrate including a cell array area and a connecting area, the connecting area including a through-silicon-via (TSV) area;

a peripheral circuit structure disposed on the substrate;

a lower conductive layer disposed on the peripheral circuit structure;

a connecting conductive layer disposed on the lower conductive layer in the cell array area;

a connecting mold layer disposed on the lower conductive layer in the connecting area;

a supporter disposed on the connecting conductive layer and the connecting mold layer;

a buried insulating layer disposed in the TSV area and extending through the lower conductive layer, the connecting mold layer and the supporter;

a lower stack disposed on the supporter, the lower stack including a plurality of lower insulating layers and a plurality of lower word lines alternately stacked with the lower insulating layers;

an upper stack disposed on the lower stack, the upper stack including a plurality of upper insulating layers and a plurality of upper word lines alternately stacked with the upper insulating layers;

a plurality of channel structures extending through the lower stack and the upper stack in the cell array area;

a plurality of dummy channel structures extending through the lower stack and the upper stack in the connecting area;

a pair of separation insulating layers extending vertically through the lower stack and the upper stack and extending in a first horizontal direction, the pair of separation insulating layers being spaced apart from each other in a second horizontal direction crossing the first horizontal direction;

a word line separation layer disposed at an upper portion of the lower stack and crossing the pair of separation insulating layers, the word line separation layer extending

vertically through at least one of the lower word lines and extending in the second horizontal direction; and

a TSV disposed in the TSV area, the TSV extending through the upper stack and the lower stack and connected to the peripheral circuit structure,

wherein the lower stack further includes a plurality of lower sacrificial layers disposed at the same level as the plurality of lower word lines in the TSV area,

wherein the TSV extends vertically through the plurality of lower sacrificial layers, and

wherein a lower surface of the word line separation layer is disposed at a higher level than a lower surface of the lower stack.