Claims

1. A failure location method for a 3D stacked packaged integrated circuit chip to be tested, characterized in that the method comprises:

- determining a plurality of contrast detection layers located at different depths in a standard sample device;
- after grinding out each contrast detection layer, carry out short-circuit failure treatment on a surface of an exposed contrast detection layer to form a failure simulation hot spot, so that the contrast detection layer is in a failure state; using a thermal imager to detect phase values corresponding to different detection frequencies of the exposed contrast detection layer in the failure state;
- determining a failure location curve of each contrast detection layer according to the corresponding relationship between detection frequency and the phase value of each contrast detection layer in the failure state detected by the thermal imager; wherein, the failure location curve is a curve in which the phase value of the contrast detection layer changes with the detection frequency;
- before determining a failure location of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curves of each contrast detection layer, further comprising:
- detecting the phase value of the 3D stacked packaged integrated circuit chip to be tested at different detection frequencies by the thermal imager; wherein, the detection frequency range of the 3D stacked packaged

integrated circuit chip to be tested is within the detection frequency range of the standard sample device; and

- determining a failure position curve of the 3D stacked packaged integrated circuit chip according to the correspondence between the detection frequency and the phase value of the 3D stacked packaged integrated circuit chip to be tested;
- determining the failure location of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each contrast detection layer; wherein the standard sample device is a 3D stacked packaged integrated circuit chip of the same type as the 3D stacked packaged integrated circuit chip to be tested; wherein
- the standard sample device is without failure; wherein the composition film layers of the standard sample device and the corresponding positions of each composition film layer are the same as the composition film layers and the corresponding positions of each composition film layer of the 3D stacked package integrated circuit chip to be tested;

whereby the composition films of different positions layers correspond to different depths;

wherein the determining of a plurality of contrast detection layers located at different depths in the standard sample device comprises:

- a plurality of contrast detection layers at different depths are determined according to functional film layers of the standard sample device;

wherein the determining the plurality of contrast detection layers located at different depths according to the functional film layers of said standard sample device comprises:

selecting alternate functional film layers of the standard sample device as the contrast detection layers;

wherein the functional film layers of the standard sample device comprise: a solder ball layer, a PCB substrate, and a first connected contact point layer, an adapter unit, a second connected contact point layer and a top-layer chip stacked in sequence;

wherein selecting alternate functional film layers of the standard sample device as the contrast detection layers comprises:

selecting the solder ball layer, the first connected contact point layer and the second connected contact point layer as the contrast detection layers.

2. The method for locating failures of 3D stacked packaged integrated circuit chip according to claim 1, wherein using the thermal imager to detect the phase values corresponding to different detection frequencies of the exposed contrast detection layer in the failure state comprises detecting the phase values of the exposed contrast detection layer at different detection frequencies using the thermal imager from a side of the standard sample device that is away from the grinding side.

3. The failure location method for a 3D stacked packaged integrated circuit chip according to claim 1, wherein the failure location of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each contrast detection layer comprises:

according to the relative distance between the failure location curve of each contrast detection layer and the failure position curve of the 3D stacked package integrated circuit chip to be tested, the position of the failure film layer of the 3D stack package integrated circuit chip to be tested is determined.

4. A failure location device for a 3D stacked packaged integrated circuit chip, characterized in that it is used to perform the failure location method for a 3D stacked packaged integrated circuit chip according to any one of claims 1-3, comprising:

- a contrast detection layer determination unit configured to determine a plurality of contrast detection layers at different depths in the standard sample device;
- a phase value detection unit being used to detect the phase values corresponding to different detection frequencies of the exposed contrast detection layer in the failure state through the thermal imager after each layer of the contrast detection layer is ground sequentially;
- the failure location curve determination unit being used to determine the failure location curve of the contrast detection layer according to the corresponding relationship between the detection frequency and the phase value of each contrast detection layer in the failure state; wherein,

the failure location curve is a curve of the phase value of the contrast detection layer as a function of the detection frequency;

- a failure location unit being used to locate the failure of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each contrast detection layer; wherein the standard sample device is of the same type of 3D stacked packaged integrated circuit chip to be tested; wherein the standard sample device is uncompromised.