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Description

Method for producing printed circuit boards having
5 coarse conductor structures and at least one region
having fine conductor structures

DE 32 45 272 A1 discloses a method for producing
miniaturized thick- and thin-film circuits in which,
10 for the purpose of significantly increasing the
conductor track density first of all at least on those
regions of the substrate at which a miniaturized
conductor track geometry is provided, a whole-area
layer of conductive material is applied and this layer
15 is then subdivided by means of a laser, which is
controlled according to a negative layout program and
is aligned with respect to the substrate, into mutually
separate partial areas and/or strips which at least in
part form a conductor track in each case. When a
20 multiplicity of IC pads are connected to a surrounding
periphery, diverging tracks burnt by the laser result
in the production of conductor tracks which diverge in
a star-shaped manner, are very narrow on the IC side
and are each assigned to one of the closely adjacent
25 pads and the widened outer ends of which are led to
periphery connections. As a result of the track burnt
by the laser being routed in the shape of a spiral,
inductances can also be formed in the layer that is
conductive in a whole-area manner. In this case, a
30 highly compact and thus space-saving inductance
structure can be obtained by the spiral arrangement of
the conductor track located in each case between two
tracks burnt by the laser.

35 EP 0 602 258 A1 discloses a method for producing
printed circuit boards having coarse conductor
structures, in which case, however, a delimited region
of these printed circuit boards is intended to obtain a
very high wiring density. This is achieved by means of

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an additional wiring layer which is applied only in the delimited region and is connected to the

underlying wiring layer via plated-through holes.

EP 0 062 300 A2 discloses a method for producing printed circuit boards in which a metallic etching resist that has been applied over the whole area of a metal layer is selectively removed again by means of laser radiation in the regions which do not correspond to the conductor structures, and the conductor structures are formed by etching away the metal layer that is uncovered in this way.

DE 41 31 065 A1 discloses a method for producing printed circuit boards in which a metal layer and a metallic or organic etching resist layer are successively applied to a substrate, whereupon said etching resist layer is removed by means of laser radiation in the regions directly adjoining the subsequent conductor track pattern, and the metal layer that is uncovered as a result is etched away in such a way that the conductor track pattern and island regions of the metal layer remain on the substrate, said island regions being electrically insulated from said conductor track pattern by etching trenches. The patterning by means of laser radiation can be performed rapidly since the regions of the etching resist layer which are to be removed only have to have a small width and the larger areas remain between two conductor tracks.

30 The invention specified in claim 1 is based on the problem of providing a method for producing printed circuit boards having a high conductor track density in at least one delimited region, which method is economical and simple to carry out.

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The invention is based on the insight that by combining conventional photoetching technology for producing the coarse conductor structures and the laser patterning for producing the fine conductor structures, the method

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sequences can be coordinated with one another in such a way that

the formation of the coarse and fine conductor structures can be performed in a common etching process.

5 In principle, the production of the fine conductor structures would also be possible using conventional photoetching technology. In this case, however, particularly high-quality photoresists, particularly high-quality light sources and particularly high-
10 quality photomasks would have to be used and the work would have to be carried out in dust-free rooms. All these measures can be obviated by the application of laser patterning for the fine conductor structures, a very high yield also being obtained at the same time.

15 For the purposes of the invention, coarse conductor structures are to be understood as those structures which have conductor track widths and conductor track spacings of more than 100 μm , whereas fine conductor
20 structures are understood to be those structures which have conductor track widths and conductor track spacings of 100 μm or less.

Advantageous refinements of the invention are specified
25 in claims 2 to 11.

The refinement according to claim 2 makes it possible to produce plated-through holes both in the region of the coarse conductor structures and in the region of
30 the fine conductor structures.

The development according to claim 3 makes it possible, through the metallic reinforcing layer, to produce extremely reliable plated-through holes in the region
35 of the coarse conductor structures.

The refinement according to claim 4 enables, as required, a particularly simple protection of the region having one conductor structures during the

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deposition of the metallic reinforcing layer in the region of the coarse conductor structures.

The refinement according to claim 5 makes it possible to pattern the photoresist with the aid of a laser beam in the region of the fine conductor structures. In accordance with claim 6, in this case an etching resist
5 can then be applied to the coarse and to the fine conductor structures particularly simply and in the desired structure in one work operation.

In accordance with claim 7, the protection of the
10 region having fine conductor structures during the application of the metallic reinforcing layer can also be effected in a simple manner by means of a temporary mask which is then simply removed again.

15 The development according to claim 8 enables direct laser patterning of the etching resist in the region of the fine conductor structures, said laser patterning being particularly simple to realize.

20 Although, in principle, organic resists, such as e.g. electro-dip coating resist, can also be used as the etching resist, in accordance with claim 9 a chemical or electrical deposition of metallic etching resists is preferred. In this case, in accordance with claim 10,
25 the use of tin or tin-lead as etching resist has proved particularly successful.

If the etching resist disturbs the further treatment of the printed circuit board, it is removed again in
30 accordance with claim 11. In this case, it is then possible for example to apply other metal layers to the coarse and to the fine conductor structures.

An exemplary embodiment of the invention is explained
35 in more detail below with reference to the drawing.

In the figures:

Figure 1 shows a plan view of a printed circuit board having coarse conductor structures and a region having fine conductor structures in a greatly simplified schematic illustration,

Figure 2 shows various method stages of a first embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures,

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Figures 3 shows various method stages of a second embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures,

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Figure 4 shows various method stages of a third embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures.

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Figure 1 shows, in a greatly simplified schematic illustration a plan view of a printed circuit board, which is designated in its entirety by LP and on the surface of which there are a region having coarse conductor structures GL, which region is only indicated by a contour line, and a delimited region B having fine conductor structures FL, which likewise cannot be discerned in any detail. There are four alignment markers JM in the corner points of the region B, which markers enable the respective devices to be positioned exactly when working in the region B.

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Figure 2 shows various method stages a to h of a first embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures. In the individual sections through an electrically insulating substrate S, the region for the coarse conductor structures is in each case situated to the left of a dotted line L, while the region of the fine conductor structures is situated to the right of said dotted line L.

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In accordance with Figure 2a, a metal layer MS is applied to the substrate S, whereupon plated-through holes DL are bored

in the region having coarse conductor structures and in the region having fine conductor structures. The metal layer MS is a copper coating, for example.

- 5 In accordance with Figure 2b, a metallization layer ME is subsequently applied to the metal layer MS and to the walls of the plated through holes DL e.g. by chemical and electrical copper deposition.
- 10 Afterwards, in accordance with Figure 2c, a photoresist PR is applied and is patterned by exposure and development in such a way that, in the region of the coarse conductor structures, it has a negative pattern of said coarse conductor structures and, on the other
- 15 hand, covers the entire region of the fine conductor structures. In accordance with Figure 2d, a reinforcing layer VS is then applied to those regions of the metallization layer ME which are not covered by the photoresist PR, and in particular in the plated-through
- 20 holes DL, e.g. by electrical copper deposition. The task of this reinforcing layer VS is to increase the reliability of the plated-through holes.

- In accordance with Figure 2e, the photoresist PR is
- 25 then patterned in the region of the fine conductor structures with the aid of a laser beam LS in such a way that it has the negative patterning of the fine conductor structures. By way of example, an Nd:YAG laser having a wavelength of 1.06 μm or 355 nm is used
- 30 for this laser patterning.

- Afterwards, in accordance with Figure 2f, an etching resist AR is applied to the coarse conductor structures and to the fine conductor structures in one work
- 35 operation. In the exemplary embodiment illustrated, the etching resist AR is applied by electrodeposition of tin.

After the removal - illustrated in Figure 2g - of the photoresist PR, the coarse conductor structures GL and the fine conductor structures FL are then produced in a common etching process

in accordance with Figure 2h. In this common etching process, those regions of the metallization layer ME and of the metal layer MS which are not protected by the etching resist AR are etched away as far as the surface of the substrate S. In a final step, the residual etching resist AR is then stripped.

Figure 3 shows various method stages a to h of a second embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures. In this case, Figures 3a and 3b correspond to Figures 2a and 2b already described.

In accordance with Figure 3c, a photoresist PR is applied to the metallization layer ME and is patterned by exposure and development in such a way that, in the region of the coarse conductor structures, it has a negative pattern of said coarse conductor structures. In the region of the fine conductor structures, a temporary mask designated by TM is applied to the metallization layer ME. Afterwards, in accordance with Figure 3d, a reinforcing layer VS is applied to the metallization layer ME in the region of the coarse conductor structures.

After the removal of the temporary mask TM in accordance with Figure 3e, an etching resist AR is then applied to the coarse conductor structures and to the region of the fine conductor structures in one work operation in accordance with Figure 3f. In the exemplary embodiment illustrated, the etching resist AR is applied by chemical deposition of tin.

In accordance with Figure 3g, the photoresist PR is subsequently removed and the etching resist AR is patterned in the region of the fine conductor structures with the aid of a laser beam LS in such a way that it has the pattern of the fine conductor

structures. An Nd:YAG laser having a wavelength of 1.06 μm is used for this laser patterning of the etching resist AR.

In accordance with Figure 3h, the coarse conductor structures GL and the fine conductor structures FL are then produced in a common etching process. In this common etching process, those regions of the metallization layer ME and of the metal layer MS which are not protected by the etching resist AR are etched away as far as the surface of the substrate S. In a final step, the residual etching resist AR is then again stripped in this case, too.

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Figure 4 shows various method stages a to h of a third embodiment of a method for producing printed circuit boards having coarse conductor structures and a region having fine conductor structures. Figures 4a and 4b correspond to Figures 2a and 2b already described.

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In accordance with Figure 4c, a photoresist PR is applied to the metallization layer ME and is patterned by exposure and development in such a way that, in the region of the coarse conductor structures, it has a negative pattern of said coarse conductor structures.

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Afterwards, in accordance with Figure 4d, a reinforcing layer VS is applied to the metallization layer ME, said reinforcing layer VS covering the entire region of the fine conductor structures in a whole-area manner.

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In accordance with Figure 4e, an etching resist AR is then applied to the reinforcing layer VS. In the exemplary embodiment illustrated, the etching resist AR is applied by chemical deposition of tin.

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In accordance with Figure 4f, the etching resist AR is subsequently patterned in the region of the fine conductor structures with the aid of a laser beam LS in such a way that it has the pattern of the fine conductor structures. An Nd:YAG laser having a wavelength of 1.06 μm is used for this laser patterning of the etching resist AR.

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After this laser patterning, the photoresist PR is removed in accordance with Figure 4g.

5 In accordance with Figure 4h, the coarse conductor structures GL and the fine conductor structures FL are then produced in a common etching process. In this case, in the region of the coarse conductor structures GL, those regions of the metallization layer ME and of the metal layer MS which are not protected by the
10 etching resist AR are etched away as far as the surface of the substrate S. In the region of the fine conductor structures FL, those regions of the reinforcing layer VS, of the metallization layer ME and of the metal layer MS which are not protected by the etching resist
15 AR are etched away as far as the surface of the substrate S. After this common etching process, the residual etching resist AR is stripped.



Patent claims

1. A method for producing printed circuit boards (LP) having coarse conductor structures (GL) and having at least one delimited region (B) having fine conductor structures (FL), having the following steps:
- a) a metal layer (MS) is applied to an electrically insulating substrate (S);
 - b) in the region of the coarse conductor structures (GL), an etching resist (AR) patterned by means of photolithography is applied to the metal layer (MS), which resist has the pattern of the coarse conductor structures (GL);
 - c) in the region (B) of the fine conductor structures (FL), an etching resist (AR) patterned with the aid of a laser beam (LS) is applied to the metal layer (MS), which resist has the pattern of the fine conductor structures (FL);
 - d) in order to form the coarse conductor structures (GL) and the fine conductor structures (FL), those regions of the metal layer (MS) which are not protected by an etching resist (AR) are etched away as far as the surface of the substrate (S) in a common etching process.
2. The method as claimed in claim 1, characterized in that, in the region of the coarse conductor structures (GL) and/or in the region of the fine conductor structures (FL), plated-through holes (DL) are introduced into the metal layer (MS) and the substrate (S), and in that a metallization layer (ME) is then applied to the metal layer (MS) and to the walls of the plated-through holes (DL).
3. The method as claimed in claim 2, characterized in that a photoresist (PR) is applied to the metallization layer (ME) at least in the region of the coarse conductor structures (GL) and is patterned by exposure and development in such a way that it has the

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negative pattern of the coarse conductor structures



(GL), and in that a metallic reinforcing layer (VS) is then applied to the metallization layer (ME).

4. The method as claimed in claim 3, characterized

5 in that the photoresist (PR) is also applied to the region (B) having fine conductor structures (FL) and covers said region during the application of the metallic reinforcing layer (VS).

10 5. The method as claimed in claim 4, characterized
in that the photoresist (PR) is patterned after the application of the metallic reinforcing layer (VS) in the region (B) having fine conductor structures (FL) with the aid of a laser beam (LS) in such a way that it
15 has the negative pattern of the fine conductor structures (LS).

6. The method as claimed in claim 5, characterized
in that the etching resist (AR) is applied to the coarse
20 conductor structures (GL) and to the fine conductor structures (FL) in one work operation, and in that the photoresist (PR) is then removed.

7. The method as claimed in claim 3, characterized
25 in that the region (B) having fine conductor structures (FL) is covered by a temporary mask (TM) during the application of the metallic reinforcing layer (VS).

8. The method as claimed in one of claims 1 to 3 or 7,
30 characterized
in that, in step c), the etching resist (AR) is applied over the whole area of the metal layer (MS) and is patterned with the aid of the laser beam (LS) in such a way that it has the pattern of the fine conductor
35 structures (FL).



9. The method as claimed in one of the preceding claims,
characterized

5 in that the etching resist (AR) is applied by chemical
or electrical metal deposition in one work operation in
the region having coarse conductor structures (GL) and
in the region (B) having fine conductor structures
(FL).

10. The method as claimed in claim 9,
10 characterized
in that tin or tin-lead is used as the etching resist
(AR).

11. The method as claimed in one of the preceding
claims,
15 characterized
in that the etching resist (AR) is removed again after
step d).