A COMPILER FOR ELABORATING HARDWARE DESCRIPTION LANGUAGE SPECIFICATIONS OF ASYNCHRONOUS DIGITAL-LOGIC SYSTEMS

Abstract

[0018] A compiler for elaborating hardware description language specifications of asynchronous digital-logic circuits into equivalent modular register-transfer level models that are suitable for HDL simulations and logic synthesis, comprising the following steps. First, a specification that is written in standard Verilog HDL and augmented by a set of compiler directives is read and analyzed. Second, internal representations of the specification are constructed by extracting the causal relations between the entities declared in the specification and establishing the communication channels that correspond to the causal relations. Third, a modular register-transfer level model equivalent to the specification is generated by inferring and instantiating the appropriate handshake modules, expanding the channels into explicit handshake signals and bundled data, interconnecting the handshake modules based on the channels, and establishing the control of the handshake modules over their respective variables.