# NONVOLATILE MEMORY WITH VARIABLE DRAIN VOLTAGE

## Field

The present invention relates generally to memory circuits, and more specifically to nonvolatile memory circuits.

## Background

Conventional nonvolatile memories include FLASH memories that utilize hot electron injection for programming Gate and drain voltages on floating gate transistors are typically elevated during the programming process. Program times for conventional FLASH memories typically increase as the parts age and the number of program/erase cycles increases.

## Brief Description of the Drawings

Figure 1 shows a floating gate transistor for use in a memory cell;

Figure 2 shows a block diagram of a memory device;

Figure 3 shows an erase cycle counter;

Figures 4 and 5 show flowcharts in accordance with various embodiments of the present invention;

Figure 6 shows drain voltage during programming versus number of erase cycles;

Figure 7 shows programming time versus number of erase cycles; and

Figure 8 shows a diagram of an electronic system in accordance with various embodiments of the present invention.

## Description of Embodiments

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that

the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein in connection with one embodiment may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

Figure 1 shows a floating gate transistor for use in a memory cell. Floating gate transistor 100 includes a channel region between drain node 102 and source node 112, and control gate 110 over the channel region. In addition, floating gate transistor 100 has a floating gate (shown schematically at 108) between the control gate and the channel region. Floating gate 108 is electrically isolated from the control gate and the channel region when nominal voltages are applied across the various terminals.

A nonvolatile memory device may have a large number of floating gate transistors arranged in arrays. In some embodiments, the control gate of each floating gate transistor is connected to a word line and the drain of each floating gate transistor is connected to a bit line. As used herein the term "nonvolatile memory" refers to a memory device that maintains its state when power is removed. Nonvolatile memories that incorporate floating gate transistors may be referred to as "FLASH" memories, although the various embodiments of the invention are not limited to those memories referred to as FLASH.

A memory cell that includes a floating gate transistor may be programmed by inducing hot electron injection from the channel region to the floating gate through the gate oxide by applying relatively high gate and drain voltages. The voltage values applied to the gate and drain of floating gate transistor 100 during

programming affect the amount of charge residing on the floating gate after programming. The amount of time that the relatively high gate and drain voltages are applied also affect the amount of charge residing on the floating gate after programming. The amount of stored charge affects current in the channel region by determining the voltage that must be applied to the gate in order to allow the floating gate transistor to conduct current between the source and the drain. This "threshold voltage" of the transistor is the physical form of the data stored in the memory cell. As the charge on the floating gate increases the threshold voltage also increases.

Over the lifetime of a memory device, floating gate transistors may be programmed and erased many times. As used herein, the term "erase cycle" refers to the process of removing stored charge on the floating gate 108. Programming time may be dependent on the number of erase cycles a floating gate transistor has undergone. For example, a memory device that has been programmed and erased only a few times may have a shorter program time than a memory device that has been programmed and erased many times.

In various embodiments of the present invention, the voltage applied to drain node 102 during programming is varied as a function of the number of previous erase cycles. For example, as the number of erase cycles increases, the drain node voltage used during programming may be increased. By increasing drain node voltage as the number of erase cycles increases, the programming time may be held more constant during the life of the memory device. Further, by providing for a lower drain voltage earlier in the life of the memory device, reliability may be increased.

Figure 2 shows a block diagram of a memory device. Memory device 200 includes write/erase control engine 210, erase cycle counter 220, variable voltage source 230, and memory blocks 240, 242, and 244. Memory blocks 240, 242, and 244 include arrays of floating gate transistors, such as floating gate transistor 100 (Figure 1). Memory blocks 240 and 244 are labeled "Block 0" and "Block $2^N$-1" to signify that $2^N$ memory blocks may be present in memory device 200.

Write/erase control engine 210 provides control signals (not shown) to various circuits within memory device 200. For example, write/erase control engine 210 may provide timing control signals to erase cycle counter 220 and variable voltage source 230. Write/erase control engine 210 may be any type of controller suitable to effect programming and erasing operations within memory device 200. For example, control engine 210 may be an embedded microprocessor, microcontroller, or the like. In operation, control engine 210 may receive and execute software instructions from a microcode store. Microcode may be held in a nonvolatile memory element. The manner in which write/erase control engine 210 is implemented is not a limitation of the present invention.

As shown in Figure 2, variable voltage source 230 provides a variable voltage on node 232 in response to information received on node 222 from erase cycle counter 220. Variable voltage source 230 may be implemented in any manner suitable to provide a plurality of different voltage values on node 232. For example, in some embodiments, variable voltage source 230 may include multiple precision voltage sources, and the output nodes of the voltage sources may be multiplexed onto node 232. In other embodiments, variable voltage source 230 generates a different output voltage using trimmable circuit elements. The manner in which variable voltage source 230 is implemented is not a limitation of the present invention.

Erase cycle counter 220 is an example of a mechanism to keep track of the number of erase cycles for each of the $2^N$ memory blocks. For example, erase cycle counter 220 may include at least one digital storage location corresponding to each of the $2^N$ memory blocks, and stored values in the digital storage locations may be incremented when the corresponding memory block is erased. The information stored in erase cycle counter 220 may be provided to variable voltage source 230 during a programming cycle, and variable voltage source 230 may provide a different voltage on node 232 based on that information.

Node 232 is coupled to the drain nodes of floating gate transistors within the memory blocks. For example, drain node 102 (Figure 1) may receive a voltage

from variable voltage source 230 on node 232. In some embodiments, node 232 may include many different physical circuit nodes or traces, and variable voltage source 230 may provide voltages to the various memory blocks on different traces.

In operation, when one of memory blocks 240, 242, or 244 is erased; erase cycle counter 220 increments a digital word maintained for the block being erased. For example, if block 240 is erased, erase cycle counter 220 will increment a digital word corresponding to block 240. In this manner, erase cycles may be counted separately for each memory block in memory device 200.

Further, during a programming operation, erase cycle counter 220 provides the erase cycle count of the block being addressed to variable voltage source 230. Variable voltage source 230 then provides a different voltage to be provided on a drain nodes of floating gate transistors based on the number of erase cycles that the addressed block has undergone.

The user address provided on node 202 is shown having components X, Y, and Z. Z includes "N" signal lines used to decode one of $2^N$ blocks. The X and Y components of the user address may be utilized to address rows and columns within a selected block.

Memory device 200 may include functional blocks and signal lines not shown in Figure 2. For example, memory device 200 may include a write interface circuit or a read interface circuit that couples various portions of memory device 200 to an external bus. Further, memory device 200 may include signal lines from one or more interface circuits to control engine 210, erase cycle counter 220, or any other block shown in Figure 2. The blocks that are shown in Figure 1 were chosen to support an explanation of various embodiments relating to the programming of the memory blocks using variable drain voltages.

In some embodiments, memory device 200 is a FLASH memory that includes arrays of multilevel cells (MLC). For example, each multilevel cell may support four different program states represented by different threshold voltages on a floating gate transistor. These four states may be represented as level zero (L0), level one (L1), level two (L2), and level three (L3), where L0 corresponds to an

unprogrammed memory cell with a lowest threshold voltage, L3 corresponds to a programmed memory cell with a highest threshold voltage, and L1 and L2 correspond to programmed memory cells with intermediate threshold voltages. L3, L2, L1, and L0 may also be represented as "00," "01," "10," and "11," respectively.

Figure 3 shows an erase cycle counter. Erase cycle counter 220 includes incrementer 320 and nonvolatile array 310. Nonvolatile array 310 is shown receiving the Z portion of the user address, read/write control information on node 312, and an incremented word on node 322. The read/write control information may be provided by write/erase control engine 210 (Figure 2).

During an erase cycle, nonvolatile array 310 receives the Z portion of the address and produces an erase cycle count on node 222 corresponding to the addressed block. Further, an incremented erase cycle count is written back to nonvolatile array 310.

During a programming cycle, nonvolatile array 310 receives the Z portion of the user address and provides the erase cycle count for the addressed block on node 222. An incremented erase cycle count is not written back to nonvolatile array 310 during a programming operation. As described above with reference to Figure 2, the erase cycle count on node 222 may be utilized to provide a different drain voltage for a particular memory block during a programming operation.

Nonvolatile array 310 may be any type of memory array capable of holding information relating to the erased cycle count of memory blocks within a memory device. For example, nonvolatile array 310 may include floating gate transistors such as floating gate transistor 100 (Figure 1). In some embodiments, nonvolatile array 310 includes one addressable location for each block of memory within a memory device. In other embodiments, nonvolatile array 310 may include multiple storage locations for each addressable memory block.

Figures 4 and 5 show flowcharts in accordance with various embodiments of the present invention. In some embodiments, methods 400 and 500 may be used to erase and program a nonvolatile memory device. In some embodiments, methods 400 and 500, or portions thereof, are performed by a controller in a nonvolatile

memory device, embodiments of which are shown in the various figures. In other embodiments, methods 400 and 500, or portions thereof, are performed by a combination of hardware and software in a nonvolatile memory device. Methods 400 and 500 are not limited by the particular type of apparatus or software element performing the method. The various actions in methods 400 and 500 may be performed in the order presented, or may be performed in a different order. Further, in some embodiments, some actions listed in Figures 4 and 5 are omitted from methods 400 and 500.

Referring now to Figure 4, method 400 is shown beginning at block 410 in which the erase cycle count of a memory block is obtained. In some embodiments, this corresponds to an erase cycle counter providing an erase cycle count for an addressed block. For example, erase cycle counter 220 (Figures 2, 3) may receive a portion of a user address, decode the block being addressed, and provide an erase cycle count for that block on node 222.

At 420, the erase cycle count is updated for the block. For example, incrementer 320 (Figure 3) may increment the erase cycle count, and the incremented erase cycle count may be written to nonvolatile memory 310 in response to the read/write information provided on node 312. At 430, the block is erased.

As described above, method 400 performs an erase of a block in a memory device and updates an erase cycle count for that block. In some embodiments, method 400 repeats the block erasure for multiple blocks, and erase cycle counts are updated for the multiple blocks.

Referring now to Figure 5, method 500 is shown beginning at block 510 in which the erase cycle count of an addressed block is obtained. As in 410 (Figure 4), the actions of block 510 may be performed when the "N" bits of an address are used to look up an erase count in a nonvolatile memory such as nonvolatile memory 310 (Figure 3).

At 520, a drain voltage for the addressed memory block is set based on the erase cycle count for the addressed block. In some embodiments, this may

correspond to variable voltage source 230 (Figure 2) setting a drain voltage on node 232 in response to an erase cycle count provided by erase cycle counter 220. At 530, the addressed block is programmed.

According the actions of method 500, the drain voltage used during programming of a memory block is increased as the number erase cycles increases for that memory block.

Figure 6 shows drain voltage during programming versus number of erase cycles. Waveform 620 represents the drain voltage used for programming. As the number of erase cycles increases, the drain voltage also increases. Waveform 620 is shown with coarse granularity and appears as a stair-step pattern. This is not a limitation of the present invention. For example, in some embodiments, many more discrete drain voltages are available, and waveform 620 appears to have smaller steps. Further, in some embodiments, waveform 620 appears almost linear. Also for example, in some embodiments, fewer discrete drain voltages are available, and waveform 620 appears as having only one two "steps" between different possible drain voltages. Waveform 610 is shown to compare a nonvariable drain voltage with the variable drain voltage of waveform 620.

Figure 7 shows programming time versus number of erase cycles. A programming time specification for a memory device is shown at 730. Programming time specification 730 is generally a published specification that a manufacturer guarantees is a maximum programming time. As shown at 710, the actual programming time increases with erase cycle count for a nonvariable drain voltage. As shown at 720, in various embodiments of the present invention, the program time is held more constant by increasing the drain voltage as the erase cycle count increases.

Waveform 720 is shown as a constant programming time, but this is not a limitation of the present invention. For example, waveform 720 may take on a "sawtooth" pattern when waveform 620 (Figure 6) has a very coarse stair-step pattern. Also for example, waveform 720 may gradually increase or decrease

depending on the characteristics of the floating gate transistors, and the characteristics of waveform 620.

Figure 8 shows a system diagram in accordance with various embodiments of the present invention. Electronic system 800 includes processor 810, nonvolatile memory device 820, memory 825, digital circuit 830, radio frequency (RF) circuit 840, and antennas 850. Processor 810 may be any type of processor adapted to access nonvolatile memory device 820 and memory 825. For example, in some embodiments, processor 810 may be a microprocessor, a digital signal processor, a microcontroller, or the like.

Example systems represented by Figure 8 include cellular phones, personal digital assistants, wireless local area network interfaces, or any other suitable system. Nonvolatile memory device 820 may be adapted to hold information for system 800. For example, nonvolatile memory device 820 may hold device configuration data, such as contact information with phone numbers, or settings for digital circuit 830 or RF circuit 840. Further, nonvolatile memory device 820 may hold multimedia files such as photographs or music files. Still further, nonvolatile memory device 820 may hold program code to be executed by processor 810. Nonvolatile memory device 820 may be any of the nonvolatile memory embodiments described herein, including nonvolatile memory device 200 (Figure 2). Many other systems uses for nonvolatile memory device 820 exist. For example, nonvolatile memory device 820 may be used in a desktop computer, a network bridge or router, or any other system without an antenna.

Radio frequency circuit 840 communicates with antennas 850 and digital circuit 830. In some embodiments, RF circuit 840 includes a physical interface (PHY) corresponding to a communications protocol. For example, RF circuit 840 may include modulators, demodulators, mixers, frequency synthesizers, low noise amplifiers, power amplifiers, and the like. In some embodiments, RF circuit 840 may include a heterodyne receiver, and in other embodiments, RF circuit 840 may include a direct conversion receiver. In some embodiments, RF circuit 840 may include multiple receivers. For example, in embodiments with multiple antennas

850, each antenna may be coupled to a corresponding receiver. In operation, RF circuit 840 receives communications signals from antennas 850, and provides signals to digital circuit 830. Further, digital circuit 830 may provide signals to RF circuit 840, which operates on the signals and then transmits them to antennas 850.

Digital circuit 830 is coupled to communicate with processor 810 and RF circuit 840. In some embodiments, digital circuit 830 includes circuitry to perform error detection/correction, interleaving, coding/decoding, or the like. Also in some embodiments, digital circuit 830 may implement all or a portion of a media access control (MAC) layer of a communications protocol. In some embodiments, a MAC layer implementation may be distributed between processor 810 and digital circuit 830.

Radio frequency circuit 840 may be adapted to receive and demodulate signals of various formats and at various frequencies. For example, RF circuit 840 may be adapted to receive time domain multiple access (TDMA) signals, code domain multiple access (CDMA) signals, global system for mobile communications (GSM) signals, orthogonal frequency division multiplexing (OFDM) signals, multiple-input-multiple-output (MIMO) signals, spatial-division multiple access (SDMA) signals, or any other type of communications signals. The present invention is not limited in this regard.

Antennas 850 may include one or more antennas. For example, antennas 850 may include a single directional antenna or an omni-directional antenna. As used herein, the term omni-directional antenna refers to any antenna having a substantially uniform pattern in at least one plane. For example, in some embodiments, antennas 850 may include a single omni-directional antenna such as a dipole antenna, or a quarter wave antenna. Also for example, in some embodiments, antennas 850 may include a single directional antenna such as a parabolic dish antenna or a Yagi antenna. In still further embodiments, antennas 850 may include multiple physical antennas. For example, in some embodiments, multiple antennas are utilized to support multiple-input-multiple-output (MIMO) processing or spatial-division multiple access (SDMA) processing.

Memory 825 represents an article that includes a machine readable medium. For example, memory 825 represents a random access memory (RAM), dynamic random access memory (DRAM), static random access memory (SRAM), read only memory (ROM), FLASH memory, or any other type of article that includes a medium readable by processor 810. Memory 825 may store instructions for performing the execution of the various method embodiments of the present invention. In operation, processor 810 reads instructions and data from either or both of nonvolatile memory device 820 and memory 825 and performs actions in response thereto. In some embodiments, nonvolatile memory device 820 and memory 825 are combined into a single memory device. For example, nonvolatile memory device 820 and memory 825 may both be include in a single nonvolatile memory device.

Although the various elements of system 800 are shown separate in Figure 8, embodiments exist that combine the circuitry of processor 810, nonvolatile memory device 820, memory 825 and digital circuit 830 in a single integrated circuit. For example, memory 825 or nonvolatile memory device 820 may be an internal memory within processor 810 or may be a microprogram control store within processor 810. In some embodiments, the various elements of system 800 may be separately packaged and mounted on a common circuit board. In other embodiments, the various elements are separate integrated circuit dice packaged together, such as in a multi-chip module, and in still further embodiments, various elements are on the same integrated circuit die.

The type of interconnection between processor 810 and nonvolatile memory device 820 is not a limitation of the present invention. For example, bus 815 may be a serial interface, a test interface, a parallel interface, or any other type of interface capable of transferring command and status information between processor 810, nonvolatile memory device 820, and memory 825.

In some embodiments, nonvolatile memory device 820 may include NOR-type FLASH memory cells, and in other embodiments, nonvolatile memory device 820 may include NAND-type FLASH memory cells. Memory cells in nonvolatile

memory device 820 may store one data bit per cell, or memory cells may be multilevel cells (MLC) capable of storing more than one bit per cell. Any memory arrangement may be utilized within nonvolatile memory device 820 without departing from the scope of the present invention.

Nonvolatile memory devices, controllers, erase cycle counters, and other embodiments of the present invention can be implemented in many ways. In some embodiments, they are implemented in integrated circuits. In some embodiments, design descriptions of the various embodiments of the present invention are included in libraries that enable designers to include them in custom or semi-custom designs. For example, any of the disclosed embodiments can be implemented in a synthesizable hardware design language, such as VHDL or Verilog, and distributed to designers for inclusion in standard cell designs, gate arrays, or the like. Likewise, any embodiment of the present invention can also be represented as a hard macro targeted to a specific manufacturing process.

Although the present invention has been described in conjunction with certain embodiments, it is to be understood that modifications and variations may be resorted to without departing from the spirit and scope of the invention as those skilled in the art readily understand. Such modifications and variations are considered to be within the scope of the invention and the appended claims.

What is claimed is:

1. An integrated circuit comprising:
a floating gate transistor cell;
a mechanism to track a number of erase cycles; and
a variable voltage source coupled to provide a drain voltage to the floating gate transistor cell, and coupled to be responsive to the mechanism to track the number of erase cycles.

2. The integrated circuit of claim 1 wherein:
the integrated circuit includes a plurality of floating gate transistor cells arranged into a plurality of blocks; and
the mechanism to track a number of erase cycles includes a plurality of storage locations to store a number of erase cycles for each of the plurality of blocks.

3. The integrated circuit of claim 1 wherein the variable voltage source is coupled to increase the drain voltage on the floating gate transistor cell as the number of erase cycles increases.

4. The integrated circuit of claim 3 wherein the floating gate transistor comprises a FLASH memory cell.

5. The integrated circuit of claim 4 wherein the FLASH memory cell comprises a NOR FLASH memory cell.

6. The integrated circuit of claim 4 wherein the FLASH memory cell comprises a NAND FLASH memory cell.

7. A memory device comprising:

a plurality of memory blocks;

an erase cycle counter to count a number of times each of the plurality of memory blocks have been erased; and

a variable voltage source to provide a variable voltage to each of the plurality of memory blocks in response to the erase cycle counter.

8. The memory device of claim 7 wherein each of the plurality of blocks includes floating gate transistors.

9. The memory device of claim 8 wherein the variable voltage source is coupled to vary a drain voltage on the floating gate transistors during programming operations.

10. The memory device of claim 9 wherein the variable voltage source is coupled to increase the drain voltage to a block as the erase cycle counter indicates a large erase cycle count.

11. The memory device of claim 7 wherein the erase cycle counter includes at least one nonvolatile storage location for each of the plurality of memory blocks.

12. The memory device of claim 7 wherein each of the plurality of memory blocks includes FLASH memory cells.

13. A method comprising:

receiving an address to address at least one memory location; and

incrementing an erase count corresponding to the at least one memory location.

14. The method of claim 13 further comprising erasing the at least one memory location.

15. The method of claim 13 further comprising setting a drain voltage on a floating gate transistor cell in the at least one memory location based on the erase count.

16. The method of claim 15 further comprising programming the at least one memory location.

17. The method of claim 15 wherein setting a drain voltage comprises setting the drain voltage to a higher value as the erase count increases.

18. An electronic system comprising:
an antenna;
radio frequency circuitry coupled to the antenna;
a processor coupled to the radio frequency circuitry; and
a memory device coupled to the processor, the memory device including a plurality of memory blocks, an erase cycle counter to count a number of times each of the plurality of memory blocks have been erased, and a variable voltage source to provide a variable voltage to each of the plurality of memory blocks in response to the erase cycle counter.

19. The electronic system of claim 18 wherein each of the plurality of blocks includes floating gate transistors.

20. The electronic system of claim 19 wherein the variable voltage source is coupled to vary a drain voltage on the floating gate transistors during programming operations.