CLAIMS

1. A method of forming a memory device, comprising:

forming a first assembly comprising a stack of alternating insulative and conductive levels over control circuitry; the first assembly including channel structures extending through the stack; the channel structures having upper and lower regions; the upper regions of the channel structures projecting above the stack; at least some of the lower regions of the channel structures being electrically coupled with bitlines and the control circuitry;

removing portions of the upper regions of the channel structures to create exposed upper regions of the channel structures; and

forming a conductive structure over the exposed upper regions of the channel structures.

2. The method of claim 1, wherein the electrical coupling to the control circuitry is through the bitlines.

3. The method of claim 1, wherein the conductive structure includes metal.

4. The method of claim 1, wherein the conductive structure includes conductively-doped semiconductor material.

5. The method of claim 4, further comprising out-diffusing dopant from the conductively-doped semiconductor material into the channel structures.

6. The method of claim 4, wherein an uppermost of the conductive levels within the stack is a source-side select gate level; and wherein the out-diffused dopant extends downwardly to at least said uppermost of the conductive levels.

7. The method of claim 4, wherein the semiconductor material comprises silicon.

8. The method of claim 4, wherein the channel structures comprise a first semiconductor material, and wherein the semiconductor material of the conductive structure is a second semiconductor material.

9. The method of claim 8, wherein the first and second semiconductor materials comprise a same semiconductor composition as one another.

10. The method of claim 8, wherein the first and second semiconductor materials both comprise silicon.

11. The method of claim 8, wherein the first and second semiconductor materials comprise different semiconductor compositions relative to one another.

12. The method of claim 1, wherein the first assembly includes memory cells along at least some of the conductive levels.

13. The method of claim 12, wherein the memory cells include charge-storage material.

14. The method of claim 1 further comprising forming an interconnect coupled with the conductive structure; the forming of the interconnect comprising:

forming an opening to pass through first and second levels and into a silicon substrate;

forming an insulative liner within the opening;

forming conductive pillar material within the opening, the silicon substrate, insulative liner and conductive pillar material together comprising a second assembly;

inverting the second assembly;

removing the silicon substrate and removing some of the insulative liner to expose a region of the conductive pillar material; and

forming the conductive structure to directly contact the exposed region of the conductive pillar material.

15. The method of claim 1, further comprising implanting a dopant into the exposed sidewalls of channel material.

16. The method of claim 1, wherein the conductive structure is against the sidewalls of the channel material.

17. The method of claim 1, wherein the conductive structure comprises a plurality of layers.

18. The method of claim 17, wherein one layer of the conductive structure comprises a metal and another layer of the conductive structure comprises a silicon layer.

19. The method of claim 1, wherein the conductive structure comprises a doped semiconductive layer.

20. The method of claim 1, wherein the conductive structure includes a metal layer and a semiconductive layer.

21. The method of claim 1, further comprising an insulative layer over the conductive structure.