

Method for machining a semiconductor wafer on both sides in a carrier, carrier and a semiconductor wafer produced by the method

5 The invention relates to a method for machining a semiconductor wafer which is guided in a cutout in a carrier while a thickness of the semiconductor wafer is being reduced to a target thickness by material being removed from a front surface and a back surface of the semiconductor wafer simultaneously. A
10 method of this type is used in particular for the double side polishing and lapping of semiconductor wafers. A carrier is used to hold and guide at least one semiconductor wafer during machining. To protect the semiconductor wafer, the cutout of the carrier in which the semiconductor wafer lies during
15 machining is lined with an inlay. A carrier of this type is formed by a carrier body and the at least one inlay.

According to US-6,454,635, during machining the semiconductor wafer acquires a bead-like thickened portion in the edge region
20 when the thickness of the inlay, as a result of wear, becomes less than the thickness of the carrier body.

US-2004/0235401 includes the description of a carrier, the inlay of which is at least 20 μm thicker than the thickness of
25 the carrier body. This is intended to prevent wear to the carrier body from releasing metals during the machining of the semiconductor wafer, which would contaminate the semiconductor wafer.

30 JP-05-177539 A proposes a method for the double side polishing of semiconductor wafers, according to which the thickness t of the semiconductor wafer to be machined, the thickness T of the carrier and the depth of penetration x of the semiconductor wafer into the polishing cloth are matched to one another
35 according to the inequality $T-2x < t < T+2x$. The method can be

used, inter alia, to produce semiconductor wafers which are concave in cross section and in which a particularly flat front surface can be generated by subsequent single side polishing.

- 5 It is desirable for the demands imposed on the flatness of the front surface of a semiconductor wafer as far as possible also to be satisfied in the edge region of the semiconductor wafer, so that this region can also be used to construct electronic components.

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The local flatness on the front surface of a semiconductor wafer is generally specified by the $SFQR_{\max}$ value. For this purpose, the area of the front surface is divided into sites, taking into account an edge exclusion, and the positive and
15 negative deviation from a reference plane is determined, the reference plane being determined for each site by error square minimization. The $SFQR_{\max}$ value (Site Frontside Site-Least-Squares Range) indicates the deviation which is not exceeded in 100% of the sites.

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It is an object of the present invention to specify a method which in technical terms is relatively simple and which provides semiconductor wafers with a local flatness of the front surface, even in the edge region, which satisfies the
25 demands imposed on this parameter for the fabrication of current and future generations of electronic components.

The object is achieved by a method for machining a semiconductor wafer which is guided in a cutout in a carrier
30 while a thickness of the semiconductor wafer is being reduced to a target thickness by material being removed from a front surface and a back surface of the semiconductor wafer simultaneously, wherein the semiconductor wafer is machined until it is thinner than a carrier body and thicker than an

inlay used to line the cutout in the carrier to protect the semiconductor wafer.

5 The primary application area of the invention is the double side polishing of semiconductor wafers, in particular of wafers which partially or completely consist of silicon.

10 The invention also relates to a semiconductor wafer which has been polished on both sides and has a front surface, a back surface and an edge R as well as a local flatness on the front surface, expressed as $SFQR_{max}$, of less than 50 nm with an edge exclusion of R - 2 mm and of less than 115 nm with an edge exclusion of R - 1 mm, these details being based on a grid with a site area of $26 * 8$ mm.

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Semiconductor wafers with a diameter of at least 200 mm, the local flatness $SFQR_{max}$ of which has the values indicated as far as the edge region indicated, were hitherto not feasible. Surprisingly, this is now achievable by carrying out the double
20 side polishing in accordance with the method described above. Unlike known methods, the semiconductor wafer is positioned in a carrier, which likewise forms part of the invention, wherein the carrier body and the inlay have different thicknesses throughout the entire duration of the machining of the
25 semiconductor wafer and the carrier body is thicker than the inlay, with the thickness difference amounting to 20 to 70 μm .

The invention is based on the discovery that two conditions need to be satisfied simultaneously in order to be able to
30 achieve an excellent local flatness even in the edge region of the front surface of the semiconductor wafer. Firstly, the machining of the semiconductor wafer on both sides must lead to the machined wafer being thinner than the carrier body. The thickness difference (target thickness of the semiconductor
35 wafer - thickness of the carrier body) is preferably in the

range from < 0 to $-6 \mu\text{m}$, preferably in the range from -1 to $-5 \mu\text{m}$. Secondly, an inlay which is thinner than the carrier body must be present between the semiconductor wafer and the carrier body. This second requirement is particularly
5 surprising since this is considered disadvantageous by the abovementioned US-6,454,635. The thickness difference (thickness of the carrier body - thickness of the inlay) amounts to 20 to 70 μm , particularly preferably 30 to 60 μm .

10 Further details of the invention are described below based on the example of the double side polishing of silicon semiconductor wafers with a diameter of 300 mm and with reference to figures.

15 Fig. 1 shows a plan view of a typical carrier with cutouts for holding three semiconductor wafers.

Fig. 2 shows an enlarged detail illustrating the relative positions of semiconductor wafer, inlay and carrier body.

Fig. 3 shows a cross section through the arrangement of carrier
20 body, inlay and semiconductor wafer between two polishing plates.

The invention can be carried out on existing installations and using existing methods for the double side polishing of
25 semiconductor wafers. The installation may be designed for one or more carriers. On account of the increased throughput, an installation for a plurality of carriers is preferred, as described for example in DE-100 07 390 A1, and in which the carriers move on a planetary orbit around the center of the
30 installation. The installation includes a lower and an upper polishing plate, which can rotate freely in the horizontal plane and are covered with polishing cloth. During the polishing, the semiconductor wafers are located in the cutouts in the carriers and between the two polishing plates, which are
35 rotating and exert a certain polishing pressure on them while a polishing abrasive is supplied continuously. The carriers are

thereby also set in motion, preferably via rotating pinned wheels which engage in teeth on the circumference of the carriers.

5 Fig. 1 shows a plan view of a typical carrier with cutouts 1 for holding three semiconductor wafers. At the circumference of the cutouts are inlays 2 which are intended to protect the edges of the semiconductor wafers, which are susceptible to breaking, in particular also from release of metals from the
10 carrier body 3. The carrier body 3 may, for example, consist of metal, ceramic, plastic, fiber-reinforced plastic or metal which has been coated with plastic or with a diamond-like carbon layer (DLC layer). However, it is preferable to use steels, particularly preferably stainless chromium steel. The
15 cutouts 1 are preferably designed to hold an odd number of semiconductor wafers with a diameter of at least 200 mm, preferably 300 mm, and thicknesses of from 500 to 1000 μm .

It is also preferable for the surface of the carrier body 3 to
20 be structured on the front surface, the back surface or both surfaces of the carrier body, in order to promote the distribution of the polishing abrasive between the carrier body, the semiconductor wafer and the upper and lower polishing cloths. Instead of or in addition to the openings shown in Fig.
25 1, the surface 4 of the carrier body (front surface and/or back surface) can be provided with structures 10 which are arranged in the form of a pattern of orthogonal trenches (XY-pattern), a rhomboid pattern, a strip pattern, a pattern of radially diverging rays or an alternative pattern. The depth of the
30 structures 10 is preferably in a range from 1 to 200 μm , with the range from 20 to 100 μm being particularly preferred. The width of the structures is preferably in a range from 0.2 mm to 10 mm, with the range from 2 to 5 mm being particularly preferred.

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The inlays 2 preferably consist of a plastic, such as polyvinyl chloride (PVC), polyethylene (PE), polypropylene (PP), polyamide (PA), polystyrene (PS), polyvinylidene difluoride

(PVDF), aramide or other polymers derived from fluorohydrocarbons. It is particularly preferable to use PA, aramide and PVDF. The inlays should be regularly replaced, in particular when they have been worn down to a certain level.

5 They can be fixedly or releasably connected to the carrier body and for this purpose can, for example, be laid, adhesively bonded or injection-molded into the cutouts. It is also advantageous for the inlays to be regularly cleaned using a cloth.

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The polishing plates of modern installations have a sufficient area for it to be possible for three or more, preferably five carriers to be placed on them. The thickness of the carrier body and the thicknesses of the group of carrier bodies used in
15 one polishing run should be as uniform as possible. Therefore, the thickness variation of the carrier body measured for example with the aid of a sensor carrying out a measurement at 13 points is preferably not greater than 5 μm , particularly preferably no greater than 2.5 μm . Within a group of carriers,
20 the mean thickness, formed from 13 measurement points of the carrier bodies, should preferably vary by no more than 3 μm , particularly preferably by no more than 2 μm .

As can be seen from Fig. 2, between the semiconductor wafer W
25 and an adjacent inner edge of the inlay 2 there is a gap 5 which allows the semiconductor wafer W to move freely within the cutout 1 and is preferably 0.1 to 2 mm, particularly preferably 0.2 to 1 mm wide. The radial width of the inlay 2, measured from the inner edge 6 to the outer edge 7, is
30 preferably 2 to 10 mm, particularly preferably 2 to 4 mm. It is also preferable for the carrier body, for the purposes of improved bonding of the inlay, to be profiled at the circumference of the cutout, particularly preferably with a dovetail profile. To produce the inlay, by way of example,
35 plastic is injected into a shaping mold, which is preferably designed in such a manner that the plastic completely fills the spaces predetermined by the profile and forms a smooth inner

edge 6 which protects the semiconductor wafer, which is susceptible to breaking, during polishing and also ensures that it is not pulled in between the carrier body 3 and one of the polishing plates.

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Fig. 3 illustrates the feature required for the invention to succeed, whereby the carrier body 3 is thicker than the inlay 2, the thickness difference amounting to 20 to 70 μm , particularly preferably 30 to 60 μm . It is also preferable for
10 the inlay 2 to be arranged centrally, resulting in equal distances from the upper and lower polishing plates (8, 9). It is, however, also possible to deviate from this arrangement, in particular if the alternative arrangement brings about advantages, as may occur for example when polishing
15 semiconductor wafers with an asymmetric edge profile. Fig. 3 shows the situation in which the semiconductor wafer W has been polished to the target thickness and the polishing is ending. According to the invention, the semiconductor wafer W is polished to a target thickness which is less than the thickness
20 of the carrier body 3 and greater than the thickness of the inlay 2. The thickness difference (target thickness of the semiconductor wafer - thickness of the carrier body) is preferably less than 0 to -6 μm , particularly preferably from -1 to -5 μm .

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The success of the invention will become clear from the comparison with the prior art presented below.

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The comparative examples (C) and examples (E) relate to the double side polishing of silicon wafers with a diameter of 300 mm and a starting thickness of 800 to 805 μm on an installation of Type AC 2000 produced by Peter Wolters (Rendsburg).

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The silicon wafers were produced in accordance with the prior art by wire sawing of a single crystal, edge rounding, surface

grinding, etching in a concentrated mixture of nitric acid and hydrofluoric acid and edge polishing.

A commercially available polyurethane polishing cloth
5 reinforced with polyethylene fibers, having a Shore hardness A of approx. 80, and a polishing fluid with an SiO_2 solids content of 4% by weight and a pH of 11 were used for the double side polishing. The contact pressure of the polishing plate was 0.15 bar and the temperature was 38°C. The front surface of the
10 silicon wafer was in this case facing toward the lower polishing plate.

Three groups of carriers (Types 1 to 3) were available for the polishing. The carrier bodies of all three types of carrier
15 were made from stainless chromium steel and had a polished surface, the set of carriers of type 3 additionally being coated with DLC. The carrier bodies each had three circular cutouts arranged at regular intervals on a circular path and lined with plastic inlays.

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The local flatness of the front surface of the polished semiconductor wafers was determined using an AFS 3220 produced by ADE.

25 As can be seen from Table 1, only the carriers of Type 2 and 3 were designed in accordance with the invention. In the case of the carriers of Type 1, the thickness difference (thickness of the carrier body - thickness of the inlay) was in a range which lies outside that covered by the invention. The local flatness
30 of the front surface was in the required range of SFQR_{max} less than 50 nm only in the case of semiconductor wafers produced in accordance with the invention. Furthermore, a back surface referenced global flatness, expressed as GBIR (Global Backside Ideal Range) of these semiconductor wafers was measured using a
35 measurement appliance of Type AFS 3220 produced by ADE. It was

less than 0.800 μm both at an edge exclusion of R - 2 mm and at an edge exclusion of R - 1 mm.

Table 1:

	Type	d_{LSK}	d_{E}	$d_{\text{LSK}} - d_{\text{E}}$	$d_{\text{Z}} - d_{\text{LSK}}$	$\text{SFQR}_{\text{max}}^2$	$\text{SFQR}_{\text{max}}^1$	GBIR
		[μm]	[μm]	[μm]	[μm]	[nm]	[nm]	[μm]
C1	1	769	770	-1	-1.7	83	101	1.03 ± 0.13
C2	1	769	768	1	-1.1	63	82	0.75 ± 0.06
C3	1	769	768	1	+3.8	50	72	0.52 ± 0.03
E1	2	769	717	52	-3.0	42	82	0.75 ± 0.06
E2	2	769	717	52	-2.1	44	72	0.51 ± 0.06
E3	2	769	717	52	-0.1	48	103	0.35 ± 0.03
C4	2	769	717	52	+3.3	58	146	0.38 ± 0.03
E4	3	773	724	49	-4.8	45	114	0.77 ± 0.04
E5	3	773	724	49	-4.0	42	112	0.57 ± 0.02
C5	3	773	730	43	-7.0	57	--	0.80 ± 0.04
C6	3	773	730	43	-8.0	61	--	0.73 ± 0.03

The GBIR values are identical for an edge exclusion of 1 mm and 2 mm.

10 The abbreviations used in the table have the following meanings:

d_{LSK} : thickness of the carrier body

d_{E} : thickness of the inlay

d_{Z} : target thickness of the silicon wafer

15 $\text{SFQR}_{\text{max}}^2$: local flatness at an edge exclusion of 2 mm, 336 sites (full and partial sites) and a site area of 26*8 mm;

$\text{SFQR}_{\text{max}}^1$: local flatness at an edge exclusion of 1 mm, 342 sites (full and partial sites) and a site area of 26*8 mm;

20 GBIR (Global Backside Ideal Range): global flatness at an edge exclusion of 2 mm.

In addition to the local and global flatness, the geometry in the edge region of the semiconductor wafers was also examined. This was done using the measurement appliance NP1 300 mm produced by KLA Tencor. In this measurement method, 360 radial cross sections are calculated from the center of the silicon wafers at intervals of 1° . The radial cross sections are then divided into 4 sectors, and the mean of the 90 radial cross sections per sector is determined. Thereafter, a third order reference line is calculated for each sector for the range R-5 mm to R-35 mm. The deviations between the mean radial cross section and the reference line are determined at positions R-3 mm, R-2 mm, R-1 mm.

The deviations from the reference line can be indicated with respect to the front surface (measurement of the front surface), with respect to the back surface (measurement of the back surface) or with respect to the sum of the deviations with respect to the front surface and the back surface (thickness measurement). In the measurement, deviations with a positive sign indicate an edge roll-up, while deviations with a negative sign indicate an edge roll-off.

The deviations in the mean cross section measured at R - 2 mm from the reference curve (thickness measurement) were within a range of $-0.040 \mu\text{m}$ to $-0.003 \mu\text{m}$. In the case of the front surface, the deviations at R - 2 mm were in the range from $-0.030 \mu\text{m}$ to $0.050 \mu\text{m}$. For the measurement of the back surface, the deviations at R - 2 mm were in the range from $-0.070 \mu\text{m}$ to $0.030 \mu\text{m}$.

The deviations between the mean cross section measured at R - 1 mm and the reference curve (thickness measurement) were within a range from $-0.020 \mu\text{m}$ to $-0.070 \mu\text{m}$. For the front surface, the deviations at R - 1 mm were in the range from $-0.050 \mu\text{m}$ to $0.040 \mu\text{m}$. For the back surface measurement, the

deviations at $R - 1$ mm were in the range from $-0.080 \mu\text{m}$ to $0.030 \mu\text{m}$.

Patent Claims:

1. Method for machining a semiconductor wafer which is guided in a cutout in a carrier while a thickness of the semiconductor wafer is being reduced to a target thickness by material being removed from a front surface and a back surface of the semiconductor wafer simultaneously, wherein the semiconductor wafer is machined until it is thinner than a carrier body and thicker than an inlay used to line the cutout in the carrier to protect the semiconductor wafer.

2. The method as claimed in claim 1, wherein the semiconductor wafer is machined until the difference between the target thickness of the semiconductor wafer and the thickness of the carrier body is < 0 to $-6 \mu\text{m}$.

3. The method as claimed in claim 1 or claim 2, wherein the semiconductor wafer is machined until material with a thickness of at least $5 \mu\text{m}$ has been removed.

4. The method as claimed in one of claims 1 to 3, wherein the semiconductor wafer is machined together with other semiconductor wafers using a set of carriers in which a mean thickness of the carrier bodies varies by no more than $3 \mu\text{m}$.

5. A carrier for holding at least one semiconductor wafer while the semiconductor wafer is being machined on both sides, comprising a carrier body with a cutout for holding the semiconductor wafer and an inlay which lines the cutout in order to protect the semiconductor wafer, wherein the carrier body and the inlay have different thicknesses throughout the entire duration of the machining of the semiconductor wafer and the carrier body is thicker than the inlay, with the thickness difference amounting to 20 to $70 \mu\text{m}$.

6. The carrier as claimed in claim 5, wherein the thickness of the carrier body varies by less than 2 μm .

7. The carrier as claimed in claim 5 or claim 6, wherein the
5 inlay is 2 to 4 mm wide.

8. The carrier as claimed in one of claims 5 to 7, wherein the dimensions of the cutout are such that there is a gap between 0.1 and 2 mm wide between a semiconductor wafer which it holds
10 and the inlay.

9. The carrier as claimed in one of claims 5 to 8, which has a structure of trenches on at least one side of the carrier body, the trenches being 1 to 200 μm deep and 0.2 to 10 mm wide and
15 forming a pattern which is selected from a group consisting of a rhombic pattern, an orthogonal pattern, a strip pattern and a radial pattern.

10. A semiconductor wafer which has been polished on both
20 sides, having a front surface, a back surface and an edge as well as a local flatness on the front surface, expressed as SFQR_{max} , of less than 50 nm with an edge exclusion of R - 2 mm and of less than 115 nm with an edge exclusion of R - 1 mm, and based on a site area of 26 * 8 mm.

25 11. The semiconductor wafer as claimed in claim 10, which has a diameter of at least 200 mm.

12. The semiconductor wafer as claimed in claim 10 or claim 11,
30 wherein the deviation between a mean cross section measured by thickness measurement at R - 2 mm and a reference line determined by regression is -0.040 μm to -0.003 μm , and the deviation at R - 1 mm is -0.070 μm to -0.020 μm .

13. The semiconductor wafer as claimed in one of claims 10 to 12, wherein the deviation between a mean cross section measured by measurement of the front surface at $R - 2$ mm and a reference line determined by regression is $-0.030\text{ }\mu\text{m}$ to $0.050\text{ }\mu\text{m}$, and the
5 deviation at $R - 1$ mm is $-0.050\text{ }\mu\text{m}$ to $0.040\text{ }\mu\text{m}$.

14. The semiconductor wafer as claimed in one of claims 10 to 13, wherein the deviation between a mean cross section measured by measurement of the back surface at $R - 2$ mm and a reference
10 line determined by regression is $-0.070\text{ }\mu\text{m}$ to $0.030\text{ }\mu\text{m}$, and the deviation at $R - 1$ mm is $-0.080\text{ }\mu\text{m}$ to $0.030\text{ }\mu\text{m}$.

15. The semiconductor wafer as claimed in one of claims 10 to 14, which has a global flatness, expressed as global thickness variation GBIR, of less than $0.800\text{ }\mu\text{m}$ at an edge exclusion of
15 $R - 2$ mm and at an edge exclusion of $R - 1$ mm.