

Claims

1. A system, comprising:

a first transceiver module comprising:

a modulator configured to receive a pretransmission signal and to modulate the pretransmission signal to generate a first complex signal;

~~an~~ a first in-phase and quadrature (I/Q) module configured to receive a ~~the~~ first complex signal and to transform the first complex signal into bit words of a predetermined size and frameworks; and

a first physical layer (PHY) device configured to receive the bit words of the predetermined size and frameworks, to transmit the bit words and frameworks over at least one cable, and to perform adaptive cancellation based, at least in part, on the transmitted bit words and frameworks to improve reception over the at least one cable by the first PHY device; and

a second transceiver module comprising:

a second PHY device configured to receive the bit words and ~~the~~ frameworks from over the at least one cable;

~~an~~ a second I/Q module configured to receive the bit words and ~~the~~ frameworks from the second PHY device of the second transceiver module and to transform the bit words to a second complex signal based, at least in part, on the frameworks;

an I/Q modulator configured to modulate the second complex signal to generate a transmit signal; and

an antenna configured to transmit the transmit signal.

~~2. The system of claim 1, wherein the first transceiver module further comprises a modulator configured to receive a pretransmission signal and modulate the pretransmission signal to generate the first complex signal.~~

~~23.~~ The system of claim ~~2~~ 1, wherein the first transceiver module further comprises a phase lock loop configured to provide a clock signal to the I/Q modulator, the clock signal being at a speed that is slower than an operation of the first PHY device of the first transceiver module to allow for addition of the frameworks by the first I/Q module of the first transceiver module.

~~3. The system of claim 1, wherein the bit words of the predetermined size are 8 bit words.~~

34. The system of claim 1, wherein the predetermined size of the bit words is based on a largest size of bit words that the first PHY device of the first transceiver module may transmit over the at least one cable.

45. The system of claim 1, wherein the first complex signal is a 12 bit stream, and the first I/Q module configured to transform the first complex signal into the bit words of the predetermined size and framewords comprises the first I/Q module configured to transform the first complex signal, which is a 12 bit stream, to 8 bit words and framewords.

56. The system of claim ~~5~~ 4, wherein the first I/Q module configured to transform the first complex signal into the bit words of the predetermined size and framewords comprises the first I/Q module configured to place 8 bits from an I component of the first complex signal into a first 8 bit word, to place 4 bits from the I component and 4 bits from a Q component of the first complex data signal into a second 8 bit word, and to place 8 bits from the Q component into a third 8 bit word.

67. The system of claim ~~6~~ 5, wherein the first I/Q module is further configured to add a frameword to the first 8 bit word and a frameword to the second 8 bit word.

78. The system of claim 1, wherein the at least one cable is a category five Ethernet cable.

89. The system of claim 1, wherein the second transceiver module further comprises:
a waveguide filter configured to filter the transmit signal; and
a waveguide module configured to provide the filtered, transmit signal from the waveguide filter to the antenna.

940. The system of claim 1, wherein the first complex signal is a QAM signal.

1044. The system of claim 1, wherein the first PHY device of the first transceiver module is further configured to initialize a connection with the second PHY device of the second transceiver module to determine an expectation of location of the framewords.

1142. A system, comprising:

a first transceiver module comprising:
~~an a first in-phase and quadrature (I/Q) module configured to receive a first complex signal, and to transform the first complex signal into bit words of a predetermined size and framewords~~ place 8 bits from an I component of the first complex signal into a first 8 bit word, to place 4 bits from the I component and 4 bits from a Q component of the first

complex signal into a second 8 bit word, and to place 8 bits from the Q component into a third 8 bit word to generate bit words of a predetermined size and frameworks; and

a first physical layer (PHY) device configured to receive the bit words of the predetermined size and frameworks, to transmit the bit words and frameworks over at least one cable, and to perform adaptive cancellation based, at least in part, on the transmitted bit words and frameworks to improve reception over the at least one cable by the first PHY device; and

a second transceiver module comprising:

a second PHY device configured to receive the bit words and ~~the~~ frameworks from over the at least one cable;

~~an~~ a second I/Q module configured to receive the bit words and ~~the~~ frameworks from the second PHY device of the second transceiver module and to transform the bit words to a second complex signal based, at least in part, on the frameworks;

a demodulator configured to demodulate the second complex signal; and

a storage device configured to store ~~the~~ data within a computer readable medium.

~~12~~13. The system of claim-~~12~~ 11, wherein the first transceiver module further comprises:

an antenna configured to receive a receiver signal; and

an I/Q demodulator configured to generate the first complex signal based on the receiver signal.

~~13~~14. The system of claim-~~13~~ 12, wherein the first transceiver module further comprises:

a waveguide module configured to receive the receiver signal from the antenna; and

a waveguide filter configured to filter the receiver signal from the waveguide module and provide the filtered, receiver signal to the I/Q demodulator.

~~14~~15. The system of claim-~~13~~ 12, wherein the first transceiver module further comprises:

a phase lock loop configured to provide a clock signal at a speed that is slower than an operation of the first PHY device of the first transceiver module to allow for ~~the~~ addition of frameworks by the first I/Q module of the first transceiver module; and

an analog-to-digital converter configured to digitally convert the first complex signal based on the clock signal from the phase lock loop.

~~16. The system of claim 12, wherein the bit words of the predetermined size are 8 bit words.~~

~~1547.~~ The system of claim ~~12~~ 11, wherein the predetermined size of the bit words is based on a largest size of bit words that the first PHY device of the first transceiver module may transmit over the at least one cable.

~~1618.~~ The system of claim ~~12~~ 11, ~~wherein the I/Q module configured to transform the first complex signal into bit words of the predetermined size and framewords comprises the I/Q module configured to transform the first complex signal, which is a 12 bit stream, to 8 bit words and framewords.~~

~~19.~~ The system of claim ~~18~~, wherein the I/Q module configured to transform the first complex signal into bit words of the predetermined size and framewords comprises the I/Q module configured to place 8 bits from an I component of the first complex signal into a first 8 bit word, to place 4 bits from the I component and 4 bits from a Q component of the first complex data into a second 8 bit word, and to place 8 bits from the Q component into a third 8 bit word.

~~20.~~ The system of claim ~~18~~, wherein the I/Q module is further configured to add a frameword to the first 8 bit word and a frameword to the second 8 bit word.

~~1721.~~ The system of claim ~~12~~ 11, wherein the at least one cable is a category five Ethernet cable.

~~1822.~~ A method comprising:

receiving a pretransmission signal and modulating the pretransmission signal to generate a first complex signal;

receiving a the first complex signal;

transforming, by a first in-phase and quadrature (I/Q) module, the first complex signal into bit words of a predetermined size and framewords;

transmitting, by a first physical layer (PHY) device, the bit words of the predetermined size and framewords over at least one cable;

performing, by the first PHY device, adaptive cancellation based, at least in part, on the transmitted bit words and framewords to improve reception over the at least one cable by the first PHY device;

receiving, by a second PHY device, the bit words and ~~the~~ framewords over the at least one cable;

transforming the bit words, by a second I/Q module, to a second complex signal based, at least in part, on the framewords;

modulating, by an I/Q modulator, the second complex signal to generate a transmit signal; and

transmitting, by an antenna, the transmit signal.

~~23. The method of claim 22, further comprising receiving a pretransmission signal and modulating the pretransmission signal to generate the first complex signal.~~

~~1924. The method of claim-23 18, further comprising~~ generating, by a phase lock loop, a clock signal and controlling the modulation of the pretransmission signal based, at least in part, on the clock signal, the clock signal being at a speed that is slower than a transmission speed of the first PHY device to allow for ~~the~~ addition of the frameworks.

~~2025. The method of claim-22 18, wherein the predetermined size is of the bit words is~~ based on a largest size of bit words that the first PHY device may transmit over the at least one cable.

~~2126. The method of claim-22 18, wherein the at least one cable is a category five Ethernet cable.~~

~~2227. A method comprising:~~

receiving a first complex signal;

transforming, by a first in-phase and quadrature (I/Q) module, the first complex signal by placing 8 bits from an I component of the first complex signal into a first 8 bit word, placing 4 bits from the I component and 4 bits from a Q component of the first complex signal into a second 8 bit word, and placing 8 bits from the Q component into a third 8 bit word to generate ~~into~~ bit words of a predetermined size and frameworks;

transmitting, by a first physical layer (PHY) device, the bit words of the predetermined size and frameworks over at least one cable;

performing, by the first PHY device, adaptive cancellation based, at least in part, on the transmitted bit words and frameworks to improve reception over the at least one cable by the first PHY device;

receiving, by a second PHY device, the bit words and ~~the~~ frameworks over the at least one cable;

transforming the bit words, by a second I/Q module, to a second complex signal based, at least in part, on the frameworks;

demodulating, by a first I/Q demodulator, the second complex signal; and

storing, by a storage device, data within the demodulated second complex signal within a computer readable medium.

~~2328~~. The method of claim-~~27~~ 22, further comprising:

receiving, by an antenna, a receiver signal; and

generating, by ~~an~~ a second I/Q demodulator, the first complex signal based on the receiver signal.

~~2429~~. The method of claim-~~27~~ 22, further comprising generating, by a phase lock loop, a clock signal and controlling the demodulation of the first I/Q demodulator based, at least in part, on the clock signal, the clock signal being at a speed that is slower than a transmission speed of the first PHY device to allow for ~~the~~ addition of frameworks.

~~2530~~. The method of claim-~~27~~ 22, wherein the predetermined size of the bit words is based on a largest size of bit words that the first PHY device may transmit over the at least one cable.

~~2631~~. The method of claim-~~27~~ 22, wherein the at least one cable is a category five Ethernet cable.

27. A system, comprising:

a first transceiver module comprising:

a first in-phase and quadrature (I/Q) module configured to receive a first complex signal, to place 8 bits from an I component of the first complex signal into a first 8 bit word, to place 4 bits from the I component and 4 bits from a Q component of the first complex signal into a second 8 bit word, and to place 8 bits from the Q component into a third 8 bit word; and

a first physical layer (PHY) device configured to receive bit words of a predetermined size and frameworks, to transmit the bit words and frameworks over at least one cable, and to perform adaptive cancellation based, at least in part, on the transmitted bit words and frameworks to improve reception over the at least one cable by the first PHY device; and

a second transceiver module comprising:

a second PHY device configured to receive the bit words and frameworks from over the at least one cable;

a second I/Q module configured to receive the bit words and frameworks from the second PHY device of the second transceiver module and to transform the bit words to a second complex signal based, at least in part, on the frameworks;

an I/Q modulator configured to modulate the second complex signal to generate a transmit signal; and

an antenna configured to transmit the transmit signal.

28. The system of claim 27, wherein the first transceiver module further comprises a modulator configured to receive a pretransmission signal and to modulate the pretransmission signal to generate the first complex signal.

29. The system of claim 28, wherein the first transceiver module further comprises a phase lock loop configured to provide a clock signal to the modulator, the clock signal being at a speed that is slower than an operation of the first PHY device of the first transceiver module to allow for addition of the frameworks by the first I/Q module of the first transceiver module.

30. The system of claim 27, wherein the second transceiver module further comprises:

a waveguide filter configured to filter the transmit signal; and

a waveguide module configured to provide the filtered transmit signal from the waveguide filter to the antenna.

31. The system of claim 27, wherein the first PHY device of the first transceiver module is further configured to initialize a connection with the second PHY device of the second transceiver module to determine an expectation of location of the frameworks.