MICROELECTRONIC DEVICE PACKAGES, STACKED MICROELECTRONIC DEVICE PACKAGES, AND METHODS FOR MANUFACTURING MICROELECTRONIC DEVICES

TECHNICAL FIELD

[0001] The present invention is related to microelectronic device packages, stacked microelectronic device packages, and methods for manufacturing microelectronic devices.

BACKGROUND

[0002] Microelectronic devices generally have a die (i.e., a chip) that includes integrated circuitry having a high density of very small components. In a typical process, a large number of dies are manufactured on a single wafer using many different processes that may be repeated at various stages (e.g., implanting, doping, photolithography, chemical vapor deposition, plasma vapor deposition, plating, planarizing, etching, etc.). The dies typically include an array of very small bond-pads electrically coupled to the integrated circuitry. The bond-pads are the external electrical contacts on the die through which the supply voltage, signals, etc., are transmitted to and from the integrated circuitry. The dies are then separated from one another (i.e., singulated) by dicing the wafer and backgrinding the individual dies. After the dies have been singulated, they are typically "packaged" to couple

the bond-pads to a larger array of electrical terminals that can be more easily coupled to the various power supply lines, signal lines, and ground lines.

[0003] An individual die can be packaged by electrically coupling the bond-pads on the die to arrays of pins, ball-pads, or other types of electrical terminals, and then encapsulating the die in a molding compound to protect it from environmental factors (e.g., moisture, particulates, static electricity, and physical impact), and to form a microelectronic device package. In one application, the bond-pads are electrically connected to contacts on an interposer substrate that has an array of ball-pads.

[0004] Electronic products require packaged microelectronic devices to have an extremely high density of components in a very limited space. For example, the space available for memory devices, processors, displays, and other microelectronic components is quite limited in cell phones, PDAs, portable computers, and many other products. As such, there is a strong drive to reduce the surface area or "footprint" of the microelectronic device on a printed circuit board. Reducing the size of the microelectronic device can be difficult because high performance microelectronic devices generally have more bond-pads, which result in larger ball-grid arrays and thus larger footprints. One technique used to increase the density of microelectronic devices within a given footprint is to stack one microelectronic device package on top of another. However, these existing stacked designs may have certain disadvantages. For example, they may require excessive space on the

substrates for interconnections, preclude separate quality control testing of the devices, or have other drawbacks.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a schematic cross-section view of a stackable microelectronic multi-die package.

[0006] Figure 2 is a schematic cross-section of two of the packages shown in Figure 1 attached together to form a stacked assembly.

[0007] Figure 3 is a schematic cross-section view of another stackable multi-die package.

[0008] Figure 4 is a schematic cross-section view of another stackable multi-die package.

[0009] Figure 5 is a schematic cross-section view of yet another stackable multi-die package.

DETAILED DESCRIPTION OF THE DRAWINGS

[0010] A microelectronic package advantageously includes two chips or dies in a single package. This provides for a space saving design. A thinner package may also be achieved with certain designs. The package may be designed so that the dies may be separately tested before being placed into a stacked assembly. The dies may optionally be placed back-to-back, to better avoid co-planarity drawbacks. In one embodiment, a microelectronic package has a first

microelectronic die electrically connecting with a first substrate, a second substrate electrically connecting with the first substrate, and a second microelectronic die electrically connecting to the second substrate. With designs where the electrical connections are made by wire bonding, one substrate is advantageously bigger than the other substrate.

[0011] The microelectronic package may be stacked or attached to another or a second microelectronic package, to form a stacked assembly. Electrical connections may be made between the two microelectronic package assemblies, by electrically connecting or linking contacts on a first substrate of one microelectronic package with contacts on a second substrate of the other microelectronic package. The stacked package can be attached to a circuit board, with electrical connections to the circuit board made through contacts on another substrate of either package.

[0012] Many specific details of several embodiments of the invention are described below with reference to forming a plurality of microelectronic devices together in a single assembly, but in other embodiments, each device can be formed separately. Several embodiments in accordance with the invention are set forth in the drawings. The drawings, however, are provided for purpose of illustration only. They are not intended as showing limits on the scope of the invention. The following text is provided to give a thorough understanding of particular embodiments of the invention. A person skilled in the art will understand, however, that the invention may have additional embodiments, or that the invention may be practiced without several of the details described or shown in the drawings.

[0013] Turning now to Fig. 1, a stackable microelectronic package 10 has a first substrate 12 having an opening or slot 14. The opening 14 may advantageously be generally centrally located in the substrate 12. A first microelectronic die or chip 18 has an active side 40 and back side 42. The active side 40 is attached to or adjoining the first substrate 12. The active side 40 of the die 18 has terminals (e.g., bond pads) electrically connecting with contacts on a second side (shown here as the top side) of the substrate 12. The terminals and contacts are typically arranged in an array. The contacts on the substrate 12 generally are electrically connected with other contacts on the first side (shown here as the bottom side) of the substrate 12, to allow the assembly 10 to electrically connect with a circuit board or other higher level assembly.

[0014] A second microelectronic die or chip 22 has a back side 42 attached to the back side of the first die 18, preferably with an adhesive 20. This attachment (as well as the other attachments described here) may be direct or indirect, i.e., with or without one or more intermediate elements between them. Each die 18 and 22 generally has one or more integrated circuits, shown schematically in dotted lines at 25. A second substrate 24 is attached to the active side 40 of the second die 22.

[0015] The first substrate 12 is larger (i.e., wider and/or longer) than the second substrate 24, meaning that as shown in Fig. 1, the first substrate 12 extends out beyond the second substrate 24. Electrical connections are made between the first and second substrates by connecting pads or contacts 34 on the top or second side of the first substrate 12 to pads or contacts 34 on the top or second side of the

second substrate 24. These connections may be made via wire bonds 26. Since the contacts 34 on the first substrate are located on areas of the first substrate 12 that extend out beyond the second substrate 24, wire bond connections between them can be made using existing techniques. The pads or contacts 34 and 38 are shown in Fig. 1 in dotted lines, enlarged and out of scale, for illustration purposes.

[0016] Electrical connections are made between contacts on the top of the second substrate 24 and terminals on the active side of the second die 22. As shown in Fig. 1, the second substrate 24 has a through opening or slot 14. Wire bonds 26, or other connecting elements, can therefore extend through the opening 14 to make connections between the second substrate 24 and the second die 22. The wire bond sequence for the second die 22 is reversed as compared to the wire bond sequence for the first die 18, so that the pin assignment will be comparable to the ball pin out.

[0017] Electrical connections between the first substrate 12 and terminals on the first die 18 may be made in the same way. The package 10 shown in Fig.1 may be symmetrical from side to side. Although the dies 18 and 22 are shown as having the same width or length, the dies may be the same, or they may be different from each other, electrically and/or mechanically. The substrates 12 and 24 may be printed circuit boards or other types of substrates for carrying the dies, and providing electrical interconnections. The pads 134 on the substrates are typically arranged in arrays to receive an equivalent or corresponding array of electrical couplers (e.g., solder balls or other solder elements). The first die 18 and first substrate 12 form a

board-on-chip construction. Similarly, the second die 22 and the second substrate 24 also form a board-on-chip construction.

[0018] After the wire bond connections 26 are made, mold compound 28 is applied over the wire bonds 26 in the areas shown in Fig. 1. The wire bonds 26, and the contacts 34 adjacent to inner or outer edges of the substrates, and the terminals on the dies that they connect to, are covered by the mold compound 28. The dies 18 and 22 may be completely enclosed or covered on all sides by the substrates and the mold compound. The lower side of the first substrate 12 advantageously is not covered by the molding compound 28, except at the wire bonds at the opening 14. Exposed contacts 38, located between the wire bond contacts 34 on the second substrate 24, are not covered by the mold compound. This leaves the exposed contacts 38 on the lower side of the first substrate uncovered, for use in making electrical connections with another package stacked onto the package 10.

[0019] The package 10 may then be tested, since all of the contacts and terminals are still accessible by test equipment. This allows defective packages to be detected and removed, before any final assembly of the packages into a stacked assembly. The stacked assemblies therefore can be made from known good assembly packages. This increases the yield during manufacture.

[0020] In uses where the package 10 is attached to a circuit board or other higher level assembly, the package 10 may be installed as oriented in Fig. 1, i.e., with the first substrate 12 on the circuit board. Electrical connections can then be made between the package 10 and the circuit board via the exposed contacts 38

linking to contacts, pads or terminals on the circuit board. Reflow solder balls 16 may be used to make these connections. Connections to a circuit board may alternatively, or additionally be made via the exposed contacts 38 on the second substrate 24, if no additional package is stacked onto the package 10. If one or more additional packages are stacked onto the package 10, as shown in Fig. 2, then connections to a circuit board may alternately or additionally be made via exposed contacts, if any, on the package at the top of the stack.

[0021] Fig. 2 shows a second package 10 stacked onto a first package 10. Solder balls or elements 16 may be used on a land grid array, to make electrical connections between the two stacked packages. Mechanical attachment of the packages 10 may be further made with adhesive between the first substrate 12 of the top package and the mold compound 28 on the lower package, and/or between the adjoining mold compound protrusions 44 shown at the center of the stacked assembly 36. The second package may be the same or different from the first package, both electrically and mechanically, so long as any necessary electrical connections between them can be made. While Fig. 2 shows a stacked assembly 36 having two packages 10, of course, the stacked assembly 36 may also have e.g., three, four, five or more packages.

[0022] Fig. 3 shows another embodiment 48 with a first die 18 on a first substrate 52 forming a chip-on-board construction. Unlike the first substrate 12 shown in Fig. 1, the first substrate 52 in Fig. 3 has no opening or slot. A spacer or epoxy pad 50 is provided on the first die 18. A second die 22 is provided on the

spacer 50. The dies may be attached to the spacer via an adhesive 20. A second substrate 24 is attached to the second die 22, forming a board-on-chip construction, similar to the second die and second substrate in Fig. 1. The spacer 50 provides space above the active surface of the first die 18, to allow for wire bonding or similar connections to be made between the first die 18 and the first substrate 52.

[0023] If the second die 22 is smaller than the first die 18, the spacer 50 can be omitted, as it is not needed for wire bonding. In this case, the second die 22 may be attached directly to the first die 18, as in Fig. 1. Connections between the first and second dies may be made by peripheral wire bonding from the second substrate bond finger to the first substrate bond finger. The wire bonding or other electrical connections between the second substrate 24 and the second die 22, and between the second substrate 24 and the first substrate 52, as well as the mold compound 28, can be made or used in the same way as in Fig. 1, as described above. The package 48 shown in Fig. 3 may be stacked onto additional other microelectronic packages (which may be the same as or different from the package 48) to form stacked assemblies 36, similar to the concept shown in Fig. 2.

[0024] Fig. 4 shows another embodiment 58 generally similar to the design shown in Fig. 3, but with the first die 60 in a flip-chip package construction. The first die 60 is attached to the first substrate 52 with the active side down. Electrical connections between the first die 60 and the first substrate 52 are made via conductive bumps or electrical couplers on the down facing active side. The bumps are aligned with, and make contact with, target pads or contacts on the first

substrate 52. The back of the second die 22 is attached to the back of the first die 60. A second substrate 24 is attached onto the active side of the second die 22, forming a board-on-chip construction. The electrical connections between the second die 22 and second substrate 24, and between the first substrate 52 and the second substrate 24, as well as the molding compound 28, may be provided in the same way as described above with reference to Figs. 1 or 3. The package 58 may be stacked to form a multiple-package stacked assembly 36, as also described above relative to Figs. 1-3.

[0025] Fig. 5 shows another embodiment 68 generally similar to the design shown in Fig. 4, but using a flip chip as the second die 60 attached to the smaller substrate 74. A first die 72 is attached to a first substrate 70, in a board-on-chip construction. The second die 60 may be attached back-to-back onto the first die 72 using an adhesive 20. A second substrate 74 is attached to the second die 60. As the second die 60 is a flip chip, electrical connections are made between the second die and the second substrate via bumps on second die, as described above with reference to the first die 60 in Fig. 4. The second substrate 74, which is attached to the second die 60, is smaller than the first substrate 70. Electrical connections between the first and second substrates, and between the first die 72 and the first substrate 70, may be made via wire bonds 26.

[0026] The designs described above may provide advantages such as avoiding co-planarity issues (since the dies are back-to-back), allowing for assembly using existing equipment, the first and second substrates can have a ball pin out

assignment conforming to industry standards (JEDEC), the components may be individually tested before final assembly, and a thinner package height may be achieved. Of course, practice of the invention in different ways, using different embodiments, may or may not realize each of these advantages. The invention may also be used without necessarily achieving each advantage.

[0027] The words pads, contacts, terminals, bumps, electrical couplers, etc. are intended to describe any features, without limitation, that are used in making electrical connections, are not intended to have specific exclusive meanings. The word attached as used here means directly or indirectly joined, adhered, linked, bonded or otherwise supported on. The word substrate here means an element or base to which a die is attached, with a substrate typically, but not exclusively, comprising a circuit board. The word between generally means a direct connection between a first element and second element, as in peripheral wire bonding, but also includes other types of direct or indirect electrical connections.

[0028] Thus, several embodiments, and the methods for making them, have been shown and described. Various changes and substitutions may be made without departing from the spirit and scope of the invention. The invention, therefore, should not be limited, except by the following claims, and their equivalents.

CLAIMS:

1. A microelectronic package, comprising:
a first substrate;
a first microelectronic die electrically connecting with the first substrate;
a second substrate electrically connecting with the first substrate; and
a second microelectronic die electrically connecting to the second substrate.

2. The microelectronic package of claim 1 further including a first set of wires connecting a second side of the first substrate to a second side of the second substrate; a second set or wires connecting a first side of the first substrate to a central area of the first microelectronic die; and a third set of wires connecting the second side of the second substrate to the second microelectronic die.

3. The microelectronic package of claim 1 wherein the first substrate is larger than the second substrate.

4. The microelectronic package of claim 3 with the first substrate is electrically connected to the second substrate via wire bonding.

5. The microelectronic package of claim 1 wherein the first microelectronic die comprises a board-on-chip package construction.

6. The microelectronic package of claim 1 wherein the second microelectronic die comprises a board-on-chip package construction.

7. The microelectronic package of claim 1 with the second substrate having an exposed grid array of electrical contacts to allow for a stacking assembly of two or more package assemblies.

8. The microelectronic package of claim 1 with the first and second microelectronic dies each having an active side including a plurality of active terminals, and a back side, and with the back side of the first microelectronic die attached to the back side of the second microelectronic die.

9. The microelectronic package of claim 1 with the first substrate having a first side and a second side, with the second side adjoining the first microelectronic die, and with the first side of the substrate having a plurality of contacts, and with the first substrate having a through opening, and further comprising wires extending from the plurality of contacts on the first side of the substrate to the first microelectronic die.

10. The microelectronic package of claim 9 with the second substrate having a first side and a second side, with the first side adjoining the second microelectronic die, and with the second substrate having a through opening, and further comprising wires extending from a plurality of contacts on the second die to the second side of the second substrate.

11. The microelectronic package of claim 2 further comprising a mold compound encapsulating the first, second and third sets of wires.

12. The microelectronic package of claim 1 with the first die adjoining the first substrate and with the second die adjoining the second substrate and with the first die adjoining the second die.

13. The microelectronic package of claim 1 with the first die electrically connected to the first die via plurality of electrical terminals on an active side of the first die in contact with a second side of the first substrate.

14. A stacked microelectronic package assembly, comprising:

a first microelectronic package, comprising:

a first substrate;

a first microelectronic die electrically connecting with the first substrate;

a second substrate electrically connecting with the first substrate; and

a second microelectronic die electrically connecting to the second substrate; and

a second microelectronic package, comprising:

a third substrate;

a third microelectronic die electrically connecting with the third substrate; and

a plurality of electrical connections between the second and third substrates.

15. The stacked microelectronic package assembly of claim 14 further comprising:

a first, second and third set of wires associated with the first microelectronic package assembly, with the first set of wires connecting a second side of the first substrate to a second side of the second substrate; the second set or wires connecting a first side of the first substrate to a central area of the first microelectronic die; and the third set of wires connecting the second side of the second substrate to the second microelectronic die;

a fourth substrate electrically connecting with the third substrate; and

a fourth, fifth and sixth set of wires associated with the second microelectronic package assembly, with the fourth set of wires connecting a second side of the third substrate to a second side of the fourth substrate; the fifth set or wires connecting a first side of the third substrate to a central area of the third microelectronic die; and the sixth set of wires

connecting the second side of the fourth substrate to the fourth microelectronic die.

16. The stacked microelectronic package assembly of claim 14 wherein the plurality of electrical connections between the first and second microelectronic package assemblies comprise solder balls between the second and third substrates.

17. The stacked microelectronic package assembly of claim 14 wherein the first substrate is larger than the second substrate.

18. A stackable multi-electronic die package, comprising:
a first die on a first substrate;
a second substrate on a second die;
a spacer between the first and second dies;
a first set of wires connecting the first die to the first substrate;
a second set of wires connecting the second substrate to the first substrate.

19. The stackable multi-electronic die package of claim 18 further comprising a third set of wires connecting the second die to the second substrate via an opening in the second substrate.

20. The stackable multi-electronic die package of claim 18 wherein the first die and first substrate comprise a chip-on-board package construction and the second die and the second substrate comprise a board-on-chip package construction.

21. The stackable multi-electronic die package of claim 18 with the first substrate larger than the second substrate.

22. A stackable multi-electronic die package, comprising:

a first substrate;

a first die on the first substrate, with the first die making electrical connections to the first substrate;

a second die attached onto the first die;

a second substrate on the second die;

a first set of wires connecting the first substrate to the second substrate; and

a second set of wires connecting the second substrate to the second die.

23. The stackable multi-electronic die package of claim 22 with the first substrate and the first die forming a flip chip package construction and with the second substrate and the second die forming a board-on-chip package construction.

24. The stackable multi-electronic die package of claim 22 further comprising a first array of contacts on a first side of the first substrate adapted to electrically connect to a substrate of a die package stacked onto the first substrate.

25. The stackable multi-electronic die package of claim 24 wherein the first set of wires connects a second side of the first substrate to a second side of the second substrate.

26. The stackable multi-electronic die package of claim 22 wherein the first substrate is larger than the second substrate.

27. The stackable multi-electronic die package of claim 22 wherein the second substrate is larger than the first substrate.

28. The stackable multi-electronic die package of claim 22 further comprising a casing covering at least part of the first and second substrates.

29. The stackable multi-electronic die package of claim 28 with the casing having an opening exposing an area of the second substrate having electrical contacts adapted to connect with a substrate of another package.

30. The stackable multi-electronic die package of claim 22 wherein the first and second sets of wires comprise wire bonds.

31. A method for manufacturing a microelectronic package, comprising:
attaching a first die to a first substrate;
attaching a second die to the first die;
attaching a second substrate to the second die;
making a first set of electrical connections between the first substrate and the second substrate;
making a second set of electrical connections between the first die and the first substrate; and
making a third set of electrical connections between the second die and the second substrate.

32. The method of claim 31 wherein the first, second and third sets of electrical connections are wire-bond connections.

33. The method of claim 31 wherein the second set of electrical connections are made via wires extending through an opening in the first substrate.

34. The method of claim 33 wherein the third set of electrical connections are made via wires extending through an opening in the second substrate.

35. The method of claim 32 further comprising enclosing the first, second and third sets of electrical connections in a mold compound.

36. The method of claim 32 with the first set of wire bonds connecting contacts on a second side of the first substrate to contacts on a second side of the second substrate.

37. The method of claim 32 with the second set of wire bonds connecting contacts on a first side of the first substrate to terminals on a first side of the first die.

38. The method of claim 32 with the third set of wire bonds connecting contacts on a second side of the substrate to contacts on a second side of the second die.

39. The method of claim 31 wherein the first substrate is larger than the second substrate.

40. The method of claim 31 wherein the first die comprises a board-on-chip package construction.

41. The method of claim 31 wherein the second microelectronic die comprises a board-on-chip package construction.

42. The method of claim 35 further comprising excluding the mold compound from areas of the second substrate to leave a grid array of electrical contacts exposed, to allow the microelectronic package to be stacked on another microelectronic package.

43. The method of claim 35 further comprising excluding the mold compound from areas of the first substrate to leave a grid array of electrical contacts exposed, to allow the microelectronic package to be stacked on another microelectronic package.

44. The method of claim 31 further comprising attaching a back surface of the first die to a back surface of the second die via an adhesive.

45. A method for manufacturing a stacked microelectronic package assembly, comprising:

making a first microelectronic package by:

attaching a first die to a first substrate;

attaching a second die to the first die;

attaching a second substrate to the second die;

making a first set of electrical connections between the first substrate and the second substrate;

making a second set of electrical connections between the first die and the first substrate; and

making a third set of electrical connections between the second die and the second substrate; and

attaching a second microelectronic package to the first microelectronic package assembly.

46. The method of claim 45 further comprising making electrical connections between the first and second microelectronic packages by connecting contacts of the second microelectronic package to contacts on the first substrate.

47. The method of claim 46 further comprising making the electrical connections between the first and second microelectronic packages via solder elements.

48. The method of claim 45 further comprising testing at least one of the first and second microelectronic packages before attaching the second microelectronic package to the first microelectronic package

49. The method of claim 45 wherein the second set of electrical connections are made via wire bonds extending through an opening in the first substrate.

50. The method of claim 45 wherein the third set of electrical connections are made via wires bonds extending through an opening in the second substrate.

51. The method of claim 45 further comprising enclosing the first, second and third sets of electrical connections in a mold compound, before attaching the second microelectronic package assembly to the first microelectronic package.

52. The method of claim 45 wherein the first substrate is larger than the second substrate, and further comprising making the first set of electrical connections by wire bonding contacts of a second side of the first substrate to contacts on a second side of the second substrate.

53. The method of claim 46 further comprising attaching a third microelectronic package to the first microelectronic package and making electrical connections between the first and third microelectronic packaged by connecting contacts of the third microelectronic package to contacts on the second substrate.

54. The method of claim 46 wherein the contacts on the first substrate are located away from the edges of the first substrate.

55. The method of claim 45 wherein the second microelectronic package is the same as the first microelectronic package assembly.

56. A method for manufacturing a microelectronic package, comprising:
attaching a first die to a first substrate;
attaching a spacer to the first die;

attaching a second die to the spacer;

attaching a second substrate to the second die;

making a first set of electrical connections between the first substrate and the second substrate;

making a second set of electrical connections between the first die and the first substrate; and

making a third set of electrical connections between the second die and the second substrate.

57. The method of claim 56 further comprising attaching a back side of the first die to a second side of the first substrate, and making the second set of electrical connections between terminals on an active side of the first die and contacts on the second side of the first substrate.

58. The method of claim 56 further comprising making the third set of electrical connections between generally centrally located terminals on an active side of the second die and contacts on a second side of the second substrate, via wires extending through an opening in the second substrate.

59. The method of claim 56 further comprising attaching a second microelectronic package to the first substrate or the second substrate.

60. A method for making a stackable multi-electronic package, comprising:

attaching a first die onto a first substrate, with the first die having electrical couplers physically contacting pads on the first substrate;

attaching second die on the first die;

attaching a second substrate on the second die;

wire bonding first contacts on the first substrate to first contacts on the second substrate; and

wire-bonding connecting terminals on the second die to second contacts on the second substrate.

61. The method of claim 60 wherein the first contacts on the first substrate are adjacent to an edge of the first substrate, and wherein the first contacts on the second substrate are adjacent to an edge of the second substrate.

62. The method of claim 60 wherein the second contacts on the second substrate are adjacent to an opening in the second substrate.