Unpolished Semiconductor Wafer and Method for Producing an Unpolished Semiconductor Wafer

The invention relates to an unpolished semiconductor wafer and to a method for producing an unpolished semiconductor wafer.

According to the prior art, semiconductor wafers are produced in a multiplicity of successive process steps, which can generally be subdivided into the following groups.

a) production of a single crystal of semiconductor material (crystal pulling);
b) separation of the semiconductor single crystal into individual wafers (wafering, sawing);
c) mechanical processing of the semiconductor wafers;
d) chemical processing of the semiconductor wafers;
e) chemical-mechanical processing of the semiconductor wafers.

Added to this, there are a multiplicity of substeps such as cleaning, measuring and packaging.

A single crystal is conventionally produced by pulling a semiconductor single crystal from a melt (CZ or Czochralski method) or by recrystallizing a rod of polycrystalline semiconductor material (FZ or floating zone method).

Wire sawing (multi-wire slicing, MWS) and internal hole sawing are known as separating methods.

In wire sawing, a multiplicity of semiconductor wafers are separated from a crystal piece in one working step. Wire saws have a wire gate which is formed by the saw wire wound around two or more wire guide rolls. The saw wire may be coated with cutting grain (diamond wire MWS). When using wire saws with a saw wire without firmly bound cutting grain, cutting grain is supplied in the form of a suspension during the separation process (slurry MWS). The wire gate, in which the saw wire is

arranged in the form of wire sections lying parallel next to one another, penetrates through the crystal piece during the separation process. The penetration of the wire gate is caused by a forward movement device, which guides the crystal piece against the wire gate or the wire gate against the crystal piece.

In internal hole sawing, a circularly round rotating saw blade which is clamped on its outer circumference in a clamp system, has a central circular bore (internal hole) and whose circumferential region is provided with a cutting coat, and the crystal piece to be cut which is fastened in a frame by means of an adapter device and is brought by an adjustment mechanism into the intended cutting position and held there, are subjected to a relative motion by which the cutting edge works radially through the crystal piece until a semiconductor wafer is finally separated.

The mechanical processing serves to remove saw corrugations, to abrade surface layers which have suffered crystalline damage by the rough sawing processes or have been contaminated by the saw wire, and above all for global planarization of the semiconductor wafers. Here, sequential single-side grinding (SSG) methods and simultaneous double-disk grinding (DDG) methods as well as lapping are used.

In single-side grinding, the semiconductor wafer is held on the rear by a support (chuck) and planarized on the front side by a cup grinding disk or, which is less customary, by an outer grinding disk with rotation of the support and the grinding disk and slow radial adjustment.

In simultaneous double-disk grinding (DDG), the freely suspended semiconductor wafer is simultaneously processed on both sides between two grinding disks mounted on opposite collinear spindles, while being guided substantially free from constraining forces axially between a water (hydrostatic principle) or air cushion (aerostatic principle) acting on the

front and rear sides and loosely prevented from floating radially through by a surrounding thin guide ring or by individual radial spokes.

Furthermore, distinction can be made between coarse grinding and fine grinding depending on the granularity and binding of the grinding disks.

In the scope of this invention, fine grinding means that grinding disks are used with synthetic resin-bonded grinding grain and an average grinding granularity of #1500 (mesh) or finer (larger mesh number).

When coarse grinding is involved, this means a grinding step using grinding disks with average grinding granularities of less than #1500.

Such grinding disks are available, for example, from Disco Corp. Japan. The average grinding granularity is specified according to Japanese Industrial Standard JIS R 6001:1998.

In lapping, while supplying a suspension containing abrasives, the semiconductor wafers are moved under a certain pressure between an upper and a lower working disk, which usually consist of steel and are provided with channels for improved distribution of the lapping agent, and semiconductor material is thereby removed. The semiconductor wafers lie in suitably dimensioned recesses of so-called rotor disks, the rotor disks being set in rotation by means of an inner and an outer drive rim and the semiconductor wafers thus being guided on a geometrical path determined by the drive parameters. The pressure is usually transmitted via a pneumatically, hydraulically or electrically operating force transmission device from the upper working disk onto the semiconductor wafers and the lapping agent lying between the working disks and the semiconductor wafers.

The edge of the semiconductor wafer, including any existing mechanical markings such as an orientation notch or an essentially rectilinear flat on the wafer edge, is usually also processed (edge notch grinding). To this end, conventional grinding steps with profiled grinding disks, belt grinding methods with continuous or periodic forward tool movement or integrated edge rounding methods (edge grinding and edge polishing in one step) are used.

The group of chemical processing steps comprises cleaning and etching steps, in particular the removal of contaminations, in order to abrade damaged surface layers and to reduce the surface roughness. Etching steps with alkaline media, particularly based on NaOH (sodium hydroxide), KOH (potassium hydroxide) or TMAH (tetramethylammonium hydroxide) and etching steps with acidic media, in particular based on mixtures of HNO_3/HF (nitric acid/hydrofluoric acid) or combinations of such etching steps are employed for etching. Other etching methods such as plasma etching are occasionally also used.

The group of chemical-mechanical processing steps comprises polishing steps by which, through partial chemical reaction and partial mechanical material abrasion, the surface is smoothed with respect to local planarity, nanotopology and surface roughness, and residual damage of the surface is removed. Polishing generally comprises one or more prepolishing (abrasion polishing) and grinding-free (fine polishing) polishing steps and optionally also intermediate steps (buff polishing).

DE 10215960 A1 describes a method for producing semiconductor wafers, in which the following process sequence is employed:
a) separating a semiconductor single crystal into wafers,
b) lapping the front and rear sides of the semiconductor wafers,
c) etching the front and rear sides of the semiconductor wafers,
d) finely grinding at least the front sides of the

semiconductor wafers,
e) etching the front and rear sides of the semiconductor wafers,
f) polishing the semiconductor wafers.

During the production of semiconductor wafers for CMOS (Complementary Metal Oxide Semiconductor) applications, final polishing of at least the front side of the semiconductor wafer as per step f) in DE 10215960 is provided in all known methods, in order to meet the stringent requirements for global and local planarity and nanotopology of starting materials for the production of these components.

For the production of semiconductor wafers for applications in power electronics or for the fabrication of discrete components, however, these methods are too elaborate and uneconomical.

Semiconductor wafers intended for such applications are therefore usually lapped and treated with an etchant after separation from a single crystal. Polishing of the semiconductor wafers is not provided in this case. Attempts are made to achieve the planarity and gloss requirements of the semiconductor wafer merely by lapping and etching.

A method with a sawing-lapping-etching process sequence is known, for example, from US 6,063,301.

A disadvantage of this method is that lapping leads to damage deep into the interior of the crystal lattice, which usually necessitates increased material abrasion during the subsequent etching in order to remove it. A high etching abrasion leads to a deterioration of the planarity of the semiconductor wafer

A sawing-etching-lapping-etching sequence is described in US 5,899,744. The material abrasion during the lapping is intended to be reduced here by already carrying out a first etching treatment of the semiconductor wafer before the lapping step.

This method is also disadvantageous since a further deterioration of the planarity of the semiconductor wafer is to be expected from two etching steps.

An inferior surface roughness of the semiconductor wafers produced, namely less than 100 nm, is reported in all known methods in which a lapping step is provided.

It is proposed in DE 10237247 A1 to separate the semiconductor wafer from a single crystal, subject the semiconductor wafer to a treatment with an etchant and subsequently clean it, no further mechanical processing steps such as grinding, lapping or polishing being provided. A gloss-etched semiconductor wafer with a reflectivity of at least 70% can be produced by this method.

The reflectivity of a semiconductor wafer is essentially determined by projecting light onto the semiconductor wafer at a particular angle (40 to 80°) and measuring the reflected component.

Semiconductor wafers with an unsatisfactory surface roughness of 0.1-0.5 µm are also disclosed in the cited documents.

Another disadvantage of this method is that even here a high etching abrasion is provided, which entails a deterioration of the planarity or a microstructure of a surface of the semiconductor wafer. This microstructure is distinguished by visually perceptible roughness variations over length scales of 50-2000 µm and is also known to the person skilled in the art as an "orange peel" structure.

Such a microstructure of the surface leads to a limitation of the possible linewidth in photolithographic processes during the production of components. This linewidth means the minimum distance between two objects of the overall component, for

example the distance between the opposing edges of two interconnects.

It is therefore an object of the invention to improve the surface quality of unpolished semiconductor wafers and permit smaller linewidths of components produced thereon.

The object of the invention is achieved by a method for producing an unpolished semiconductor wafer, which comprises the following steps: (a) pulling a single crystal of a semiconductor material, (b) grinding the single crystal round, (c) separating a semiconductor wafer from this crystal, (d) rounding the edge of the semiconductor wafer, (e) surface-grinding at least one side of the semiconductor wafer, (f) treating the semiconductor wafer with an etchant, (g) finally cleaning the semiconductor wafer.

According to step (a) of the method according to the invention, a single crystal of semiconductor material is first produced by the crystal pulling method.

The single crystal is in this case preferably produced according to the FZ method.

The method is also equally suitable for crystals pulled by means of CZ.

Silicon is preferably used as the semiconductor material.

A single crystal preferably has a 1-0-0, 1-1-0 or 1-1-1 crystal orientation.

A single crystal is preferably doped by adding a dopant to the single crystal during the pull.

The single crystal is preferably p- or n-doped and has a resistance of 0.001-100000 Ohmcm, with a resistance variation of less than ±10% in the axial and radial directions.

In the case of a p–doped single crystal, a 1-0-0 single crystal pulled by means of FZ is for example gassed with diborane during the pull and a resistance value of 50 Ohmcm is achieved.

Subsequently, according to step (b) of the method according to the invention, the single crystal is ground round according to the prior art.

The diameter of the single crystal ground round is preferably 75-300 mm.

A semiconductor wafer is subsequently separated from the roundly ground single crystal according to step (c).

The separation of the semiconductor wafer from the single crystal is preferably carried out by means of a wire saw according to the prior art.

Nevertheless, separation of the semiconductor wafer from the single crystal by an internal hole saw is also preferred.

For the production of a semiconductor wafer with a thickness of 700 µm or more, separation of this semiconductor wafer by an internal hole saw is more economical and therefore particularly preferred over wire sawing.

The edge of the semiconductor wafer is subsequently rounded according to (d).

The edge of the semiconductor wafer is in this case preferably given a circular shape in cross section, which is usually characterized by two parameters: on the one hand by the circle radius and on the other hand by an angle which a tangent of the circle, at a point where the circle line intersects a line parallel to the surface of the semiconductor wafer, makes with that line.

At least the front side of the semiconductor wafer is subsequently ground according to step (e).

The rear side of the semiconductor wafer is preferably also ground.

After the grinding, the semiconductor wafer thus either has a ground front side and a sawed rear side or it is ground on both sides.

The material abrasion is preferably selected so that surface damage caused by the separation of the semiconductor wafer from the single crystal is completely removed.

The grinding of the semiconductor wafer is preferably carried out sequentially in the case of grinding on both sides.

Simultaneous double-disk grinding (DDG) is also preferred.

The grinding in this case respectively comprises two steps: coarse grinding and subsequent fine grinding of one side (the front side) or both sides (front and rear sides) of the semiconductor wafer.

The coarse grinding is preferably carried out by grinding disks with a grinding agent granularity of #100-1000.

Grinding disks with a grinding agent granularity of #2000-8000 are preferably used for the fine grinding.

A material abrasion during the coarse grinding preferably lies in the range of 5-100 µm, preferably in the range of 20-60 µm on one side of the semiconductor wafer.

During the fine grinding, the material abrasion is preferably in the range of 2-50 µm, preferably in the range of 5-20 µm on one side of the semiconductor wafer,

If the semiconductor wafer is separated by means of an internal hole saw in step (c) of the method according to the invention, it is preferable to grind the semiconductor wafer on both sides in step (e). If only the front side of a semiconductor wafer separated by means of an internal hole saw would be ground, this could mean that the greater crystalline damage below the surface of the semiconductor wafer (subsurface damage) on the rear side of the semiconductor wafer compared to wire sawing is not completely removed by the subsequent treatment with an etchant, and residual damage remains on the rear side of the semiconductor wafer, which forms into larger defects during a process in the component production, particularly during a thermal process, and could therefore cause impairment of the function of the components and in the worst case their failure.

After the surface grinding, the semiconductor wafer is treated with an etchant according to step (f) of the method according to the invention.

This removes the subsurface damage remaining from the grinding step in the case of grinding the semiconductor wafer on both sides, and the subsurface damage remaining because of the grinding on one side and the sawing on the other side of the semiconductor wafer in the case of single-side grinding.

The semiconductor wafer is preferably treated with an acidic etchant.

The material abrasion during the treatment of the semiconductor wafer with the acidic etchant is preferably 5-100 µm on each side of the semiconductor wafer.

A material abrasion of 10-20 µm on each side of the semiconductor wafer is preferred.

The etching step is preferably carried out with a mixture of HF/HNO_3 (hydrofluoric acid/nitric acid).

HF/HNO_3 is particularly well suited for removing metallic contaminations caused by previous mechanical processing steps (wire sawing, grinding) from the surface of the semiconductor wafer.

Washing steps with distilled water, wet chemical hydrophilization preferably carried out by means of H_2O/O_3 (water/ozone) and a drying step are furthermore preferred in the scope of step (f).

The hydrophilization is preferably carried out in a gas phase by means of O_3 gassing after drying the semiconductor wafer.

Native oxide is formed on both sides of the semiconductor wafer by the hydrophilization, so that the surface of the semiconductor wafer is sealed and the risk of creating imprints during subsequent contact with handling equipment is reduced.

This native oxide layer is preferably 0.5-3 nm thick.

A measurement of planarity parameters (for example global planarity GBIR) and the thickness of the semiconductor wafer is preferably carried out after the treatment of the semiconductor wafer with the etchant according to (f).

It is furthermore preferable to determine bulk resistance values of the semiconductor wafer.

This has the advantage that a semiconductor wafer which does not lie in a determined tolerance range with respect to its planarity and/or its resistance can be rejected.

It is furthermore preferable to calibrate the semiconductor wafers into groups with a particular resistance and/or a defined thickness.

Since contact of the semiconductor wafer to be analyzed with the material transporting the semiconductor wafer (typically

polyurethane, for example) occurs during the measurements or handling of the semiconductor wafer, and despite the hydrophilicity of the surfaces of the semiconductor wafer, a certain contamination of the semiconductor wafer cannot be ruled out, for example in the form of an imprint on the semiconductor wafer (for example of a conveyor belt or a chuck, i.e. a support suitable for holding a semiconductor wafer), in the form of particles or else as metallic contamination (primarily by direct contact with a conveyor belt), or by cross-contamination from a previous measurement process on a semiconductor wafer with a not yet cleaned, still contaminated surface, a subsequent cleaning step to remove those particles and imprints on the semiconductor wafer is necessary after the measurements.

Final cleaning of the semiconductor wafer is therefore carried out in step (g) of the method according to the invention.

The cleaning preferably involves a sequence: cleaning the semiconductor wafer in baths of surfactants - washing - treatment in aqueous HF solution (optionally with O_3) to remove metallic contaminations - further hydrophilicization, which is carried out either wet chemically or by gassing - and drying the semiconductor wafer.

The treatment in aqueous HF solution removes metallic contaminations, which may be caused by previous measurements and by handling equipment, from the surfaces of the semiconductor wafer.

The concentration of the aqueous HF solution is preferably 0.2-5%.

In order to be able to identify visually perceptible defects and reject a semiconductor wafer having such defects, a visual inspection of the semiconductor wafer is preferably carried out after the final cleaning.

The semiconductor wafer can subsequently be packaged and prepared for dispatch.

A particular advantage of the method according to the invention is that it is a less expensive method than the prior art of producing a polished semiconductor wafer, but a surface quality of the semiconductor wafer produced thereby is nevertheless achieved which corresponds essentially to that of a polished semiconductor wafer. This is achieved according to the invention by replacing the hitherto customary lapping by a grinding step.

The semiconductor wafer produced by the method according to the invention has a surface roughness of 3 nm or less on its at least one ground and etched side, which represents a significant improvement over the prior art of a "sawed, lapped and etched semiconductor wafer" (roughness 100 nm or more).

A relatively low etching abrasion is required in the method according to the invention compared to the production method of a sawed, lapped and etched semiconductor wafer, the effect of which is to avoid a deterioration of the microstructure of the semiconductor wafer with high etching abrasions ("orange peel").

At the same time, planarity parameters are achieved which are better than the prior art of a "sawed, lapped and etched semiconductor wafer".

Furthermore, it is also possible to produce thin semiconductor wafers with a thickness of 80-100 µm by the method according to the invention, which is not possible with a sawing-lapping-etching process sequence according to the prior art.

The object of the invention is also achieved by an unpolished semiconductor wafer having a front side and a rear side, wherein at least its front side is ground and its front and rear sides are etched, which has a reflectivity of 95% or more

at least on its front side, a surface roughness of 3 nm or less at least on its front side, a thickness of 80-2500 µm, a global planarity value GBIR of 5 µm or less, which is based on an edge margin of 3 mm and which has a photolithographic resolution of up to 0.8 µm, and which furthermore contains a native oxide layer with a thickness of 0.5-3 nm respectively on its front and rear sides.

The thickness of the semiconductor wafer corresponds to the respective requirements for the component process, and is preferably 100-500 µm.

The global planarity value GBIR is preferably 0.5-3 µm.

The semiconductor wafer is preferably a monocrystalline silicon wafer.

The global planarity relates to the entire surface of the semiconductor waiter less an edge margin to be defined, and is described by a global planarity value GBIR (global backsurface-referenced ideal plane/range = magnitude of the positive and negative deviation from a backsurface-referenced ideal plane for the entire front side of the semiconductor wafer), which corresponds to the previously customary specification TTV (total thickness variation).

The photolithographic resolution of at least 0.8 µm is intended to mean that the semiconductor wafer according to the invention is suitable for the production of electronic components with linewidths of up to 0.8 µm by means of photolithography.

The semiconductor wafer according to the invention preferably has a reflectivity of 98% or more at least on its front side.

The semiconductor wafer according to the invention preferably has no damage, craters, plastic residue or other defects that can be identified by means of a visual inspection.

Furthermore, preferably no particles are visible on the semiconductor wafer according to the invention under visual observation with collimated light.

The rear side of the semiconductor wafer is preferably likewise ground and etched.

The semiconductor wafer according to the invention furthermore preferably has 10^{13} cm^{-2} or less, preferably 5×10^{8}-10^{13} cm^{-2} of metallic contaminations with measurement by means of VPD-TXRF (vapor phase decomposition-total reflection X-ray fluorescence analysis) or VPD-ICP-MS (inductively coupled plasma with quadrupole mass spectrometer).

The metal contaminations are preferably copper, nickel or calcium contaminations.

The semiconductor wafer is preferably of the p or n conduction type and has a 1-0-0, 1-1-0 or 1-1-1 crystal orientation in its bulk, a resistance range of 0.001-100000 Ohmcm and a resistance tolerance of less than ±10%.

The 0.5-3 nm thickness of the native oxide is preferably measured on the semiconductor wafer according to the invention by means of ellipsometry.

The semiconductor wafer preferably has a circular shape of its edge in cross section, which is characterized on the one hand by the circle radius and on the other hand by an angle which a tangent of the circle, at a point where the circle line intersects a line parallel to the surface of the semiconductor wafer, makes with that line.

Example:

The following process parameters were selected for the production of semiconductor wafers:

Wire sawing to thickness 425 µm; grinding abrasion 50 µm per side, of which 30 µm by coarse grinding and 20 µm by fine grinding; etching treatment with a material abrasion of 12.5 µm per side.

This gave the following parameters of the semiconductor wafers produced:

- GBIR 1.5 µm ± 1 µm;

- Thickness 300 µm ± 10 µm;

- Reflectivity: 99% ± 0.7%;

- Short-range surface roughness, measured by means of AFM (atomic force microscope), length scales up to 50 µm: 3 nm ± 1 nm;

- Long-range surface roughness (on length scales up to 2 mm): 30 nm ± 3 nm (orange peel);

- Edge shape: edge circle radius of 150 µm and a tangent angle of 32°.

Patent Claims

1. A method for producing an unpolished semiconductor wafer, which comprises the following steps: (a) pulling a single crystal of a semiconductor material, (b) grinding the single crystal round, (c) separating a semiconductor wafer from this crystal, (d) rounding the edge of the semiconductor wafer, (e) surface-grinding at least one side of the semiconductor wafer, (f) treating the semiconductor wafer with an etchant, (g) finally cleaning the semiconductor wafer.

2. The method as claimed in claim 1, wherein the single crystal according to (a) is pulled by the FZ method.

3. The method as claimed in claim 1, wherein the single crystal according to (a) is pulled by CZ method.

4. The method as claimed in one of claims 1 to 3, wherein the crystal has a 1-0-0, 1-1-0 or 1-1-1 crystal orientation and silicon is used as the semiconductor material.

5. The method as claimed in one of claims 1 to 4, wherein a dopant is added to the single crystal during the pull.

6. The method as claimed in one of claims 1 to 5, wherein a diameter of the single crystal after grinding round is 75-300 mm.

7. The method as claimed in one of claims 1 to 6, wherein the separation of the semiconductor wafer from the single crystal according to (c) is carried out by means of a wire saw.

8. The method as claimed in one of claims 1 to 6, wherein the separation of the semiconductor wafer from the single crystal is carried with an internal hole saw.

9. The method as claimed in one of claims 1 to 8, wherein the surface grinding according to (e) comprises coarse grinding by grinding disks having a grain size of #100-1000 (mesh) with material abrasion of 5-100 µm, and fine grinding by grinding disks having a grain size of #2000-8000 (mesh) and a material abrasion of 2-50 µm.

10. The method as claimed in claim 9, wherein the material abrasion is 20-60 µm in the coarse grinding and 5-20 µm in the fine grinding.

11. The method as claimed in one of claims 1 to 10, wherein the front and rear sides of the semiconductor wafer are ground in the surface grinding of the semiconductor wafer according to (e).

12. The method as claimed in claim 11, wherein the surface grinding of the semiconductor wafer is carried out sequentially.

13. The method as claimed in claim 11, wherein the surface grinding of the semiconductor wafer is carried out simultaneously on both sides.

14. The method as claimed in one of claims 1 to 13, wherein an acid etchant is used in the treatment of the semiconductor wafer according to (f), and a material abrasion during it is 5-100 µm.

15. The method as claimed in claim 14, wherein the material abrasion is 10-20 µm.

16. The method as claimed in claim 14 or 15, wherein a mixture of HF/HNO_3 is used as the etchant.

17. The method as claimed in one of claims 14 to 16, wherein step (f) furthermore comprises washing steps with distilled

water, wet chemical hydrophilization of the semiconductor wafer and a drying step.

18. The method as claimed in claim 17, wherein the hydrophilization is carried out by means of O_3 gassing after drying the semiconductor wafer.

19. The method as claimed in one of claims 1 to 18, wherein a measurement of planarity parameters and the thickness of the semiconductor wafer as well as a determination of bulk resistance values are carried out after the treatment of the semiconductor wafer with the etchant according to (f).

20. The method as claimed in claim 19, wherein the semiconductor wafer is rejected if it does not lie in a determined tolerance range with respect to its planarity or its resistance.

21. The method as claimed in claim 19, wherein the semiconductor wafer is calibrated into a group with a particular resistance.

22. The method as claimed in claim 19 or 21, wherein the semiconductor wafer is calibrated into a group with a particular thickness.

23. The method as claimed in one of claims 1 to 22, wherein the final cleaning of the semiconductor wafer according to (g) comprises cleaning the semiconductor in baths of surfactants, washing, treatment in aqueous HF solution, hydrophilization which is carried out either wet chemically or by gassing, as well as drying the semiconductor wafer.

24. The method as claimed in one of claims 1 to 23, wherein a visual inspection of the semiconductor wafer is carried out after the final cleaning of the semiconductor wafer according to (g).

25. An unpolished semiconductor wafer having a front side and a rear side, wherein at least its front side is ground and its front and rear sides are etched, which has a reflectivity of 95% or more at least on its front side, a surface roughness of 3 nm or less at least on its front side, a thickness of 80-2500 µm, a global planarity value GBIR of 5 µm or less, which is based on an edge margin of 3 mm and which has a photolithographic resolution of up to 0.8 µm, and which furthermore contains a native oxide layer with a thickness of 0.5-3 nm respectively on its front and rear sides.

26. The unpolished semiconductor wafer as claimed in claim 25, which is a monocrystalline silicon wafer.

27. The unpolished semiconductor wafer as claimed in claim 25 or 26, which has no damage, craters, plastic residue or other defects that can be detected by means of a visual inspection.

28. The unpolished semiconductor wafer as claimed in one of claims 25 to 27, on which no particles are visible under visual observation with collimated light.

29. The unpolished semiconductor wafer as claimed in one of claims 25 to 28, wherein the rear side of the semiconductor wafer is likewise ground and etched.

30. The unpolished semiconductor wafer as claimed in one of claims 25 to 29, which contains metallic contaminations in a concentration of 10^{13} cm^{-2} or less.

31. The unpolished semiconductor wafer as claimed in one of claims 25 to 30, which is of the p or n conduction type and has a 1-0-0, 1-1-0 or 1-1-1 crystal orientation in its bulk, a resistance range of 0.001-100000 Ohmcm and a resistance tolerance of less than ±10%.