06 JUN 2002

USING INTELLIGENT BRIDGES WITH PICO-CODE TO IMPROVE INTERRUPT RESPONSE

ABSTRACT

A computer system (30) having an improved method of handling interrupts associated with I/O operations to reduce interrupt latencies. The computer system (30) includes one or more processing units (32), a memory device (34) connected to the processing unit via a system bus (38), and a plurality of I/O devices providing interrupt sources, connected to the processor via an I/O bus (40) and a bus bridge (42). The bus bridge (42) has incorporated therein or connected thereto means (44) for intercepting interrupt requests and handling the interrupt requests without suspending the current process in the processing unit (32). In the preferred embodiment, the means (44) for intercepting and handling the interrupts includes a storage device (46) or array having pico-code instructions which are schedules for execution in a sequencer by the interrupt control logic. If the pico-code sees an interrupt that it is not programmed to handle, it can pass that interrupt to the appropriate processing unit (32) for handling.

Fig. 2

G00002