

**POWER AMPLIFIER AND LINEARIZATION TECHNIQUES
USING ACTIVE AND PASSIVE DEVICES**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to US Provisional Patent Application No. 61/394,787, filed October 20, 2010.

FIELD OF THE INVENTION

[0002] The present invention generally relates to power amplifier design, and more particularly relates to power amplifier design linearization techniques suited for any non-linear power amplifier circuits and linearization techniques for non-class-A power amplifier circuits, including Class AB, B, C or Class F power amplifiers.

BACKGROUND OF THE DISCLOSURE

[0003] The interest in high level circuit integration and multi-standard communication systems has been a motivating force behind the development of wideband power amplifiers (PAs). Unfortunately, the usable output power and efficiency of a power amplifier degrade severely as the channel bandwidth and the operation frequencies increase. The requirement of linearity is vital in PAs, even with non-constant amplitude modulation schemes, such as QPSK, OFDM and QAM, because they have fluctuating envelopes and high peak to average ratio. The non-linearity of the power amplifier also causes spectrum regrowth as well as intermodulation distortion (IMD), which leads to inter-symbol interference (ISI) and deteriorates bit error rate (BER) in high speed digital communications. Consequently, wireless communication technologies require high linear power amplifier designs to

enable the non-constant modulation techniques. Several prior art schemes have been proposed for linearization of power amplifiers. Backoff from P1dB point, predistortion, feedback and feed forward are the most commonly employed schemes.

[0004] "Backoff" biases the power amplifier so that the transmitted signal is much smaller than the maximum signal that the power amplifier is able to handle. Thus, the transmitted signal remains in the linear amplifying region. Backoff, however, is essentially paid for by increased power dissipation of the amplifying devices, more wasted power from the power supply, and the cost to implement the transmitter: all of which are limitations to mobile wireless applications.

[0005] The second commonly used method is predistortion. Predistortion consists of the insertion of a set of predistorters in the input of the nonlinear devices to be linearized. Minimization of the total intermodulation power is employed to linearize the bandpass response of the amplifier. In most cases, the predistortion is implemented in a digital technique where the analog input signal is converted to the digital format by an A/D converter. The converted digital signal data is then input to the digital signal processor (DSP) for predistortion in a sample-by-sample manner in accordance with the inverse transfer function of the power amplifier. Finally, the processed data is converted back to an analog signal by a D/A converter to serve as the predistorted input to the power amplifier for amplification. This technique offers high suppression of intermodulation distortion. But the high complexity to implement this technique, the integration issues of the silicon area required and the dissipated power limit the application of this technology.

[0006] The third method is the feedback technique which exhibits a lower complexity and offers a reasonable intermodulation distortion suppression. In the feedback method, the distortion of the output signal in both amplitude and phase

format is sensed and fed-back negatively to the input so that the combination of the original signal and the feedback signal cancel the intermodulation distortion effect. However, the application of this method is limited due to the inherent stability considerations in implementing any feedback system in radio frequency applications.

[0007] A further known method is the technique of feed forward linearization. Feed forward linearization employs a scaled down version of the power amplifier so that the output is subtracted from its input to generate an error signal as the distortion. The error signal is then amplified and combined with the main power amplifier's output to cancel the distortion of the PA. This method does not suffer from stability problems and gives good IMD suppression. However, a major drawback of the feed forward technique is high complexity, leading to high cost and sensitivity to temperature and process variations.

[0008] Additional conventional methods employ the structures of transmitters and implement the linearization across the whole transceiver structure: in the baseband stage, the IF stage and the power amplifying stage. Yet these methods also add complexity, cost and additional silicon requirements to the transceiver design and implementation.

[0009] Thus, what is needed is an efficient power amplifier design and implementation which maintains stability, linearity and usable output power while suppressing IMD without increasing cost, complexity and silicon area required. Furthermore, other desirable features and characteristics will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and this background of the disclosure.

SUMMARY

[0010] According to the Detailed Description, a power amplifier linearization technique is provided. The designed high linear power amplifier includes first second and third passive devices and an active amplifying device. The first passive device performs input matching and network biasing. The active amplifying device has parameters tuned to predetermined harmonic frequencies. The second passive device suppresses harmonic frequencies other than predetermined harmonic frequencies. And the third passive device performs output matching and network biasing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to illustrate various embodiments and to explain various principles and advantages in accordance with the present invention.

[0012] FIG. 1 illustrates a block diagram of a linear power amplifier utilizing cut-off frequency techniques and loaded linearization stub filtering of harmonics in accordance with a present embodiment.

[0013] FIG. 2 illustrates an exemplary integrated circuit layout view of the amplifying device of FIG. 1 in accordance with the present embodiment.

[0014] FIG. 3 is a graph illustrating the adjustability of the cut-off frequency of the transistor in response to biasing of the transistor collector current, I_c , in accordance with the present embodiment.

[0015] FIG. 4 is a graph illustrating the maximum oscillation frequency of the transistor as adjusted by the biasing of the transistor collector current, I_c , in accordance with the present embodiment.

[0016] FIG. 5 is a graph illustrating the cut-off frequency of the transistor as adjusted by the biasing of the transistor collector-emitter voltage, V_{ce} , in accordance with the present embodiment.

[0017] FIG. 6 is a graph illustrating the maximum oscillation frequency of the transistor as adjusted by the biasing of the transistor collector-emitter voltage, V_{ce} , in accordance with the present embodiment.

[0018] FIG. 7 is a graph illustrating the cut-off frequency of the transistor in relation to the transistor size in accordance with the present embodiment.

[0019] FIG. 8 is a graph illustrating the maximum oscillation frequency of the transistor in relation to the transistor size in accordance with the present embodiment.

[0020] FIG. 9 is a graph illustrating the S_{21} of the transistor at different cut-off frequencies in accordance with the present embodiment.

[0021] FIG. 10 illustrates a top planar view of a structure including a loaded linearization stub and an open stub and its loaded elements in accordance with the present embodiment.

[0022] FIG. 11 illustrates a top planar view of a structure of a loaded linearization stub, an open stub and its loaded elements, and a coupling element in accordance with a first alternate embodiment.

[0023] FIG. 12 illustrates a top planar view of a symmetric configuration of the loaded linearization stub in accordance with a second alternate embodiment.

[0024] FIG. 13 illustrates a top planar view of a differential drive configuration of the loaded linearization stub in accordance with a third alternate embodiment.

[0025] FIG. 14 illustrates a top, right, front perspective view of a vertical structure of the open stub and its loaded elements wherein each of the loaded elements is

implemented in different metal layers and located on both sides of the open stub in accordance with an alternate embodiment of the present embodiment.

[0026] FIG. 15 illustrates a top, right, front perspective view of a horizontal structure of the open stub and the loaded elements wherein each of the loaded elements is implemented in the same metal layer and located on both sides of the open stub in accordance with an alternate embodiment of the present embodiment.

[0027] FIG. 16 illustrates a top, right, front perspective view of a vertical structure of the open stub and the loaded elements wherein each of the loaded elements is implemented in different metal layers and located on one side of the open stub in accordance with an alternate embodiment of the present embodiment.

[0028] FIG. 17 illustrates a top, right, front perspective view of a structure of the open stub and the loaded elements wherein each of the loaded elements is implemented in different metal layers with vertical or horizontal offset in accordance with an alternate embodiment of the present embodiment.

[0029] And FIG. 18 illustrates a top, right, front perspective view of a horizontal structure of the open stub and the loaded elements wherein all of the loaded elements are implemented in the same metal layer and located on one side of the open stub in accordance with an alternate embodiment of the present embodiment.

[0030] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures illustrating integrated circuit architecture may be exaggerated relative to other elements to help to improve understanding of the present and alternate embodiments.

DETAILED DESCRIPTION

[0031] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any theory presented in the preceding background of the invention or the following detailed description.

[0032] A high linear power amplifier is provided to attenuate the harmonics produced by non-linear amplifying devices. The linearization techniques for a millimeter-wave power amplifier comprises an amplifying device with properly selected size and current or voltage biasing to achieve a cut-off frequency at second order harmonics of an interested working frequency and a loaded linearization stub attached to the amplifying device to absorb the second, third and even higher order harmonics.

[0033] The high linearization power amplifier is composed of several blocks. An input matching circuit accepts an input signal from an source. A voltage or current biasing circuit, which can be part of the input matching circuit, is used to drive the amplifying device. The amplifying device has three terminals: one is connected to ground, one is connected to a second terminal of the input matching circuit, and the other is connected to the loaded linearization stub. A choke block feeds a voltage power source to the third terminal of the amplifying device so that it provides high impedance. The linearization stub attached to the amplifying device filters out the harmonics to pass clean fundamental amplified frequencies to an output matching circuit. The output matching circuit delivers linearized output signals to a load.

[0034] Referring to FIG. 1, a block diagram 100 of the high linear power amplifier employing the linearization techniques of properly selected size and current or voltage

biasing to set the device at the required cut-off frequency or maximum oscillation frequency is depicted.

[0035] The input signal to the amplifier is applied to an input port 11 which is connected to an input matching and biasing circuit 12 including first passive devices. The proper biasing voltage or current is asserted through the biasing circuit 12 to drive an amplifying device 13 so that the cut-off frequency of the active amplifying device 13 is set at the second order harmonics of a working or desired frequency. The active amplifying device 13 may have three terminals: one is connected to ground, one is connected to a second terminal of the input matching circuit 12, and a third is connected to a loaded linearization stub 15.

[0036] A choke block 14 feeds a voltage power source 18 to the third terminal of the amplifying device 13, thereby providing high impedance to the output of the amplifying device. Second passive devices 15 are attached to the amplifying device to filter out the harmonics and to pass the clean fundamental amplified frequencies to third passive devices for an output matching circuit 16 which delivers the linearized output signals to the load through output port 19.

[0037] The second passive devices 15 can be absorbed into the third passive devices for output matching 16. The techniques of the active and passive devices in elements 12, 13, 15 and 16 are disclosed in the present embodiment. The amplifying device applicable to the high linear power amplifier in FIG. 1 includes a III-V based HEMT, a MESFET and various HBT transistors, a MOSFET, a SOI transistors, and a wide-band gap transistors, such as in GaN and SiC materials.

[0038] Referring to FIG. 2, an exemplary integrated circuit layout view 200 of the amplifying device of FIG. 1 in accordance with the present embodiment is depicted. The view 200 shows the layout of an HBT SiGe process high linear power amplifier.

[0039] A graph 300 in FIG. 3 shows that the cut-off frequency or unit current gain frequency (f_T) is adjustable by the biasing of transistor collector current, I_c . At a given collector-emitter voltage, V_{ce} , and a given transistor size, the cut-off frequency increases with the collector current, as shown by trace 31, or the cut-off frequency increases to a maximum value before dropping when the biasing collector current increases, as shown by trace 32 in FIG. 3.

[0040] Referring to FIG. 4, a graph 400 shows that maximum oscillation frequency (f_{max}) is adjustable by the biasing of transistor collector current, I_c . At a given collector-emitter voltage, V_{ce} , and a given transistor size, the maximum oscillation frequency increases with the collector current, as shown by trace 41 in FIG. 4. Alternatively, the maximum oscillation frequency increases to a maximum value before dropping when the biasing collector current increases, as shown by trace 42.

[0041] FIG. 5 depicts a graph 500 that shows the cut-off frequency is adjustable by the biasing of transistor collector-emitter voltage, V_{ce} . At a given base current biasing, and a given transistor size, the cut-off frequency increases with the collector-emitter voltage, as shown by traces 51 and 52. The graph 600 of FIG. 6 also shows that the maximum oscillation frequency is adjustable by the biasing of transistor collector-emitter voltage, V_{ce} . At a given base current biasing, and a given transistor size, the maximum oscillation frequency increases with the collector-emitter voltage, as shown by traces 61 and 62.

[0042] Graph 700 of FIG. 7 shows that the cut-off frequency is adjustable by the transistor size. At a given base current and collector-emitter voltage biasing, the cut-off frequency decreases with the increasing of collector-emitter voltage, as shown by traces 71 and 72. Referring to FIG. 8, a graph 800 shows that the maximum oscillation frequency is also adjustable by the transistor size. At a given base current

and collector-emitter voltage biasing, the maximum oscillation frequency decreases with the increasing of collector-emitter voltage, as shown by traces 81 and 82. By adjusting the base or collector current, collector-emitter voltage and transistor size, it is feasible to select the proper cut-off frequency and maximum oscillation frequency for the transistor to fit the linearization requirement in the present embodiment.

[0043] The graph 900 of FIG. 9 shows a comparison of the S21 parameter of one active amplifying device with $f_T = 180\text{GHz}$ in trace 91 and another active amplifying device with $f_T = 120\text{GHz}$ in trace 92. It can be seen from graph 900 that the attenuation in the second order and third order harmonics of the active amplifying device with $f_T = 180\text{GHz}$ is larger than that of the active amplifying device with $f_T = 120\text{GHz}$.

[0044] A first circuit implementation of an embodiment of a loaded linearization stub design 1000 in accordance with the present embodiment is shown in FIG. 10. The loaded linearization stub design 1000 can be connected to the amplifying transistor to further improve linearization performance in accordance with the present embodiment. The loaded linearization stub 1000 is composed of one or several cascaded unit elements 101 and 102 each of which can function at the same harmonic frequency or different order harmonic frequencies. In each unit element, there is a main transmission line 106 connecting between a non-linear RF signal input and a linear RF signal output, and an open stub 103 to notch filter the unwanted harmonic frequency signals. To shrink the length of the open stub 103, one or more loaded elements 104 and 105 can be added. The open stub 103 and the loaded elements 104 and 105 form multiple-stage (M stages, where M is an integer) coupled transmission

lines, which present even mode impedance and electric length, Z_{ij0e} and Θ_{ij0e} , as well as odd mode impedance and electric length, Z_{ij0o} and Θ_{ij0o} .

[0045] A further circuit implementation 1100 of a disclosed embodiment of the loaded linearization stub design is shown in FIG. 11. The implementation 1100 can also be connected to the amplifying transistor to further make linearization performance better in the present embodiment. The loaded linearization stub is composed of one or several cascaded unit elements 111 and 112, each of which can function at the same harmonic frequency or different order harmonic frequencies. In each unit element 111, 112, there is a main transmission line 116, coupling element 113 connecting between the non-linear RF signal input and the linear RF signal output, and an open stub 113 to notch filter the unwanted harmonic frequency signals. The coupling element 113 can be a capacitor or a coupling transmission line. To shrink the length of the open stub 113, one or more loaded elements 114 and 115 can be added. The open stub 113 and the loaded elements 114, 115 form multiple-stage (M stages, where M is an integer) coupled transmission lines, which present both even mode impedance and electric length, Z_{ij0e} and Θ_{ij0e} , and odd mode impedance and electric length, Z_{ij0o} and Θ_{ij0o} .

[0046] FIG. 12 depicts a symmetric configuration 1200 of the embodiment of the loaded linearization stub design in FIG. 10. The symmetric configuration similarly applies to the disclosed embodiment of the design in FIG. 11.

[0047] FIG. 13 shows a differential drive configuration 1300 for differential drive circuit applications of the embodiment of the loaded linearization stub design of FIG. 10. The configuration for differential drive application would also be applicable to the disclosed embodiment of the design in FIG. 11.

[0048] From FIG. 14 to FIG. 18, several top, right, front perspective views 1400, 1500, 1600, 1700, 1800 depict implementation examples for the passive devices of the present embodiment. Any of these implementations 1400, 1500, 1600, 1700, 1800 may use, but are not limit to the use of, a SiGe process. For example, any of these implementations 1400, 1500, 1600, 1700, 1800 may use other IC processes such as CMOS, GaAs or InP. The implementations 1400, 1500, 1600, 1700, 1800 may be based on a microstrip type structure for the stub and connection transmission lines, but the stub and connection transmission lines may also be implemented through using conventional coplanar waveguides (CPW) or conductor-backed waveguides (CPW). In FIGs. 14 to 18, the metal layers shown as dark and gray regions may be any metal layers or between any two metal layers, such as in an isolate substrate such as SiO₂, silicon.

[0049] A first implementation 1400 of the open stub and its loaded elements in FIG. 10 in microstrip structure for the present invention is shown in FIG. 14, where all the elements are fabricated in different metal layers in standard SiGe 1P6M process. In the implementation 1400, the loaded elements 141 and 143 are located in the metal layers 6 and 4, respectively, while the open stub 142 is fabricated in metal layer 5. The loaded elements have one of the ends connected to ground 144. The implementation 1400 may be modified to different configurations. For example, 141, 142 and 143 may use other metal layers or a different order of the metal layers. Also, the bottom ground may be formed as a different kind of patterned ground.

[0050] A further implementation 1500 of the open stub and its loaded elements in microstrip structure in accordance with the present embodiment is shown in FIG. 15, where all the elements are fabricated in the same metal layer in a standard SiGe 1P6M process. In the implementation 1500, the loaded elements 151 and 153 and the open

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stub 152 are fabricated in metal layer 6. The loaded elements have one of the ends connected to the ground 154.

[0051] A further implementation 1600 of the open stub and its loaded elements in microstrip structure is shown in FIG. 16, where all the elements are fabricated in different metal layers in a standard SiGe 1P6M process. In the implementation 1600, the loaded elements 162 and 163 are located in the metal layers 5 and 4, respectively, while the open stub 161 is fabricated in metal layer 6. The loaded elements have one of the ends connected to the ground 164.

[0052] Another implementation 1700 of the open stub and its loaded elements in microstrip structure is shown in FIG. 17, where all the elements are fabricated in different metal layers in a standard SiGe 1P6M process but with vertical or horizontal position offset. In the implementation 1700, the loaded elements 171 and 172 are located in metal layers 6 and 5, while the open stub 173 is fabricated in metal layer 4. The loaded elements are to the left of the open stub and have one of the ends connected to the ground 174. However, implementation 1700 is not limited to this one version--the loaded elements can be located to the right of the open stub and in upper metal layers, or the loaded elements can be located to the left of the open stub and in lower metal layers, or the loaded elements can be located to the right of the open stub and in lower metal layers.

[0053] A further implementation 1800 of the open stub and its loaded elements in microstrip structure for the present invention is shown in FIG. 18, where all the elements are fabricated in the same metal in a standard SiGe 1P6M process. In the implementation 1800, the loaded elements 182 and 183 and the open stub 181 are fabricated in metal layer 6. The loaded elements are to the right of the open stub and

have one of the ends connected to ground 184. In a similar implementation, the loaded elements can be located to the left of the open stub.

[0054] Thus it can be seen that an efficient power amplifier design and implementation which maintains stability, linearity and usable output power while suppressing IMD without increasing cost, complexity and silicon area required has been provided. Further, improved linearization techniques for a millimeter-wave power amplifier include selecting an amplifying device with proper size and current or voltage biasing to achieve a cut-off frequency at second order harmonics of an interested working frequency and connecting it to a loaded linearization stub to absorb the second, third and even higher order harmonics. While several exemplary embodiments have been presented in the foregoing detailed description of the invention, it should be appreciated that a vast number of variations exist, including variations as to the materials used to form the various layers of the magnetic recording medium.

[0055] It should further be appreciated that the exemplary embodiments are only examples, and are not intended to limit the scope, applicability, dimensions, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing an exemplary embodiment of the invention, it being understood that various changes may be made in the function and arrangement of elements and method of play steps described in an exemplary embodiment without departing from the scope of the invention as set forth in the appended claims.

CLAIMS

What is claimed is:

1. A power amplifier comprising:
a first passive device for input matching and network biasing;
an active amplifying device having parameters tuned to predetermined harmonic frequencies;
a second passive device for suppression of harmonic frequencies other than the predetermined harmonic frequencies; and
a third passive device for output matching and network biasing.
2. The power amplifier in accordance with Claim 1 wherein the first passive device is coupled to receive an input high frequency signal and perform biasing of one or more of current and voltage of the input high frequency signal, and wherein the third passive device coupled to receive a power supply current and matches an output RF signal to a load of the high linear power amplifier.
3. The power amplifier in accordance with either of Claims 1 or 2 wherein the active amplifying device is tuned to the predetermined harmonic frequencies in response to tuning intrinsic parameters of the active amplifying device including a cut-off frequency and a maximum oscillation frequency thereof.
4. The power amplifier in accordance with any of Claims 1 to 3 wherein the active amplifying device tunes the intrinsic parameters thereof by asserting a

group of proper values for a collector current, a collector-emitter voltage and a transistor size of the active amplifying device necessary to produce a predetermined gain at a fundamental frequency of the input high frequency signal and suppress harmonic frequencies of the input high frequency signal.

5. The power amplifier in accordance with any of Claims 1 to 4 further comprising a loaded linearization stub coupled to the active amplifying device, wherein the loaded linearization stub comprises one or more cascaded unit elements operating at one or more of the predetermined harmonic frequencies and different orders of the predetermined harmonic frequencies.

6. The power amplifier in accordance with any of Claims 1 to 5 wherein the one or more cascaded unit elements are connected to one another by one or more devices selected from the group of devices including transmission lines, inductors and capacitors.

7. The power amplifier in accordance with either Claim 5 or 6 wherein each of the one or more cascaded unit elements comprises a main transmission line, an open stub with a first end connected to the main transmission line, and one or more loaded elements, wherein each of the one or more loaded elements having a first end openended and a second end connected to ground.

8. The power amplifier in accordance with any of Claims 5 to 7 wherein the loaded elements can be located at one or more positions relative to the open stub selected from the group of relative positions comprising (a) a position left and a

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position right of the open stub, (b) a position above and a position below the open stub,
and (c) and positions to the same side of upper, lower, left and right of the open stub.

9. The power amplifier in accordance with any of Claims 1 to 5 wherein each of the one or more cascaded unit elements comprises a main transmission line, a coupling element, an open stub, and one or more loaded elements.

10. The power amplifier in accordance with Claim 9 wherein the coupling element is selected from the group comprising a metal-insulator-metal capacitor, a poly-insulator-poly capacitor, a MOS capacitor, a MOS varactor, a p-n varactor, an inter-digital capacitor, other capacitive coupling elements, edge-coupled lines, and broad side coupled lines.

11. The power amplifier in accordance with either Claim 9 or Claim 10 wherein the open stub has a first end open-ended and a second end connected to ground, and wherein the open stub is coupled to the main transmission line and the one or more loaded elements to form an electromagnetic field for generating a loading effect to reject unwanted nonlinearity spurious signals while enabling a compact size and a resonating effect of the power amplifier.

12. The power amplifier in accordance with any of Claims 7 to 11 wherein the transmission line, including the main transmission line, is selected from the group comprising microstrip lines, coplanar waveguides, and strip lines.

13. The power amplifier in accordance with any of Claims 7 to 12 wherein

a shape of the transmission line, including a shape of the main transmission line, is selected from the group comprising meander-lines, folded lines, spiral lines, and fish bone lines.

14. The power amplifier in accordance with any of Claims 7 to 13 wherein the open stub and the loaded elements are selected from the group comprising microstrip lines, coplanar waveguides, and strip lines, and other structures of transmission lines.

15. The power amplifier in accordance with any of Claims 7 to 14 wherein an impedance across the loaded linearization stub has an impedance value of substantially 50 Ohms.

16. The power amplifier in accordance with any of Claims 1 to 15 wherein the active amplifying device operates at a frequency of 10 GHz and above.

17. The power amplifier in accordance with any of Claims 1 to 16 wherein the active amplifying device comprises one or more devices selected from the group comprising a III-V based HEMT, a MESFET, a HBT transistor, a MOSFET, a SOI transistor; a GaN wide-band gap transistor, and a SiC wide-band gap transistor.

18. The power amplifier in accordance with any of Claims 1 to 17 wherein the power amplifier comprises a non-class A power amplifier, including Class AB, Class B, Class C, and Class F power amplifiers.

19. The power amplifier in accordance with any of Claims 1 to 18 wherein the input high frequency signal is selected from the group comprising an RF signal, a microwave signal and a millimeter-wave signal.

20. The power amplifier in accordance with any of Claims 1 to 19 wherein the active amplifying device and the second passive device utilize intrinsic high space loss of the harmonic frequencies and the active amplifying device utilizes transistor improvement techniques in response to the input high frequency signal having a frequency in the range of 10 GHz and above.

21. The power amplifier in accordance with Claim 20 wherein operational frequencies for the first, second and third passive devices are the operational frequencies both below and above 10 GHz.