

METHOD FOR REMOVING SILICON DIOXIDE FROM WAFER AND MANUFACTURING PROCESS FOR INTEGRATED CIRCUIT

TECHNICAL FIELD

The present disclosure relates to the field of manufacturing process of an integrated circuit, and in particular, relates to a method for removing silicon dioxide from a wafer applied in the manufacturing method for an integrated circuit and a manufacturing method for an integrated circuit using the method.

BACKGROUND

In the field of a manufacturing method of an integrated circuit, currently a silicon-based material is generally used to manufacture an integrated circuit, when silicon (or polycrystalline silicon) is placed in air, its surface will be naturally oxidized such that a compact layer of silicon dioxide (SiO_2) is formed, as shown in Fig. 1a. In some processes, for example, in a metal silicide process, a metal nickel-platinum (NiPt) thin film needs to contact directly with a substrate made of silicon-based material, and if there is a SiO_2 layer on the surface of the substrate, resistivity will be increased and performance of a device will be affected, hence, the SiO_2 layer needs to be removed before performing any subsequent process. While removing the SiO_2 layer, other film/structure should be protected from being removed or damaged, as shown in Fig. 1a, a line width of an isolation layer (spacer, made of silicon nitride (Si_3N_4)) will influence electrical property of the device, such as an increase in electric leakage. Therefore, SiO_2 needs to be removed while protecting the isolation layer (spacer, Si_3N_4) from being removed.

As shown in Fig. 1b, the existing processes mostly employ methods such as wet etching, plasma dry etching and the like to remove SiO_2 , which may have a low etch selectivity ratio relative to Si_3N_4 , and remove too much of the isolation layer, causing decrease in size of the isolation layer, thereby increasing electric leakage and affecting device performance.

Thus, it is necessary to develop a method having high selectivity ratio and high

efficiency for removing silicon dioxide from a wafer applied in a manufacturing method for an integrated circuit.

Information disclosed in the background of the present invention is intended merely to deepen understanding of general background technology of the present invention, and should not be construed as admitting or implying in any form that the information constitutes the prior art already well known by those skilled in the art.

SUMMARY

The present invention provides a method, applied in manufacturing method for an integrated circuit, for removing silicon dioxide from a wafer, which achieves removal of silicon dioxide with high selectivity ratio and high efficiency, by causing a gaseous etchant to directly react with silicon dioxide under a high pressure, and extracting a reaction product after the reaction.

According to an aspect of the present invention, there is provided a method for removing silicon dioxide from a wafer, including: introducing dehydrated hydrogen fluoride gas and dehydrated alcohol gas into a process chamber; mixing the dehydrated hydrogen fluoride gas and the dehydrated alcohol gas to generate a gaseous etchant; causing the etchant to react with a wafer in the process chamber, and maintaining a high pressure in the process chamber to increase etch selectivity ratio; and extracting a reaction product from the process chamber.

Optionally, a pressure in the process chamber is in a range of 30Torr to 300Torr.

Optionally, the pressure in the process chamber is 200Torr.

Optionally, a temperature in the process chamber is in a range of 20°C to 80°C.

Optionally, the temperature in the process chamber is 40°C.

Optionally, a flow rate of the hydrogen fluoride gas is in a range of 100sccm to 500sccm, and a flow rate of the alcohol gas is in a range of 100sccm to 1000sccm.

Optionally, the flow rate of the hydrogen fluoride gas is in a range of 150sccm to 225sccm, and the flow rate of the alcohol gas is in a range of 200sccm to 450sccm.

Optionally, a ratio of the flow rate of the hydrogen fluoride gas to the flow rate of

the alcohol gas is 0.8:1 to 1.2:1.

Optionally, the ratio of the flow rate of the hydrogen fluoride gas to the flow rate of the alcohol gas is 1:1.

Optionally, the alcohol gas is at least one of C₁ to C₈ monohydric alcohol gas.

Optionally, the alcohol gas is at least one of methanol, ethanol, and isopropyl alcohol.

As another aspect, the present invention further provides a manufacturing method for an integrated circuit, including the method for removing silicon dioxide from a wafer according to any one of the above-described solutions of the present invention.

Optionally, the manufacturing method includes a sub-process of profile modulation in a shallow trench isolation layer (STI) using a high aspect ratio process (HARP). In the sub-process, first, the HARP is performed to deposit STI HARP deposits with a certain thickness using CVD process, afterwards, the method for removing silicon dioxide from a wafer is employed to perform an etching operation on the STI to enlarge its opening, and the HARP and the etching operation are repeatedly performed until the manufacturing method ends.

Optionally, the manufacturing method includes a sub-process for removing a SiO₂ natural oxide layer on a hard mask layer of the STI, wherein the hard mask layer of the STI is Si₃N₄. In the sub-process, the SiO₂ natural oxide layer on a surface of the hard mask layer of the STI is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO₂ natural oxide layer relative to the STI HARP deposits is controlled, such that the SiO₂ natural oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is avoided.

Optionally, the manufacturing method includes a sub-process for removing a pad oxide layer, wherein the pad oxide layer is a SiO₂ layer formed by oxidation at a surface of a substrate by heating, which is a buffer layer for a hard mask layer of Si₃N₄ of the STI. In the sub-process, the pad oxide layer is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits is controlled, such that the pad oxide

layer is removed rapidly, and excessive etching of the STI HARP deposits is avoided.

Optionally, the manufacturing method includes a sub-process for removing a SiO₂ natural oxide layer on a silicon substrate before depositing silicon germanium. In the sub-process, the SiO₂ natural oxide layer on the silicon substrate is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO₂ natural oxide layer relative to polycrystalline silicon is controlled, such that the SiO₂ natural oxide layer is removed rapidly, and excessive damage to the silicon substrate is avoided.

Optionally, the manufacturing method includes a sub-process for removing SiO₂ natural oxide layers on a surface of a substrate and on a surface of a polycrystalline silicon gate before depositing silicide. In the sub-process, the SiO₂ natural oxide layers on the surface of the substrate and on the surface of the polycrystalline silicon gate are etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO₂ natural oxide layers relative to polycrystalline silicon is controlled, such that the SiO₂ natural oxide layers are removed rapidly, and excessive damage to the silicon substrate is avoided.

Optionally, the manufacturing method includes a STI recess sub-process in 2D NAND memory manufacturing method, wherein the NAND memory includes: a floating gate and graphically intensive area STI HARP deposits located in a graphically intensive area; and a control switch gate and graphically sparse area STI HARP deposits located in a graphically sparse area, the floating gate and the control switch gate are made of polycrystalline silicon, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are made of silicon dioxide. In the sub-process, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the STI HARP deposits relative to the floating gate or relative to the control switch gate is controlled, such that the STI HARP deposits are removed rapidly, and excessive damage to the floating gate and the control switch gate is avoided.

The method for removing silicon dioxide from a wafer and the manufacturing method for an integrated circuit according to the present invention have the following advantages:

The methods of the present invention employs a gas phase etching process to remove silicon dioxide from a wafer, compared to a wet etching process or a plasma dry etching process in the prior art, the present invention removes SiO_2 by chemical reaction, no solid reaction product is generated in the removing process, thus, the reaction product can be easily pumped out by a pump, so as to keep cleanness inside the chamber, and reduce or even eliminate particle contamination caused by the reaction product. Moreover, because the method of the present invention produces no solid reaction product, unlike the prior art, there is no need to vaporize or liquefy the solid reaction product by heating at a high temperature before discharging it, thus the methods of the present invention do not require high-temperature heating, and accordingly do not require a cooling step corresponding to the heating step, which means a simple reaction process, as such, not only can process efficiency and process capacity be improved, but also can process cost corresponding to heating and cooling steps be saved.

Further, the methods provided by the present invention employ high-pressure process (for example, 50Torr to 300Torr), and can increase an etch selectivity ratio of SiO_2 relative to Si_3N_4 (or polycrystalline silicon, HARP deposits, or the like), which can not only improve efficiency of removing silicon dioxide on a wafer, but also reduce damage to substrate.

Similarly, the manufacturing method for an integrated circuit according to the present invention employs the method of the present invention to remove silicon dioxide from a wafer, therefore, compared to the manufacturing method for an integrated circuit in the prior art which employs a wet etching or a plasma dry etching to remove silicon dioxide, the manufacturing method for an integrated circuit according to the present invention can also improve efficiency of removing silicon dioxide on a wafer, reduce damage to substrate, keep the cleanness inside the chamber, reduce or even eliminate particle contamination caused by reaction product, and at the

same time has characteristics such as simple reaction process, high process efficiency and process capacity, and low cost.

The methods of the present invention have other characteristics and advantages, these characteristics and advantages will be apparent from or described in the following specific implementations taken in conjunction with the accompanying drawings, these accompanying drawings and specific implementations together serve to explain particular principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Through more detailed description of exemplary implementations of the present invention in conjunction with the accompanying drawings, the above and other purposes, characteristics and advantages of the present invention will become more apparent, and in the exemplary implementations of the present invention, same reference signs usually denote same components.

Fig. 1a illustrates a schematic diagram of an integrated circuit device having a natural oxide layer.

Fig. 1b illustrates a schematic diagram showing an effect of removing silicon dioxide according to a method of the prior art.

Fig. 2 illustrates a flow chart of steps of a method for removing silicon dioxide on a wafer according to the present invention.

Fig. 3 illustrates a schematic diagram of an effect of the method for removing silicon dioxide on a wafer according to the present invention.

Figs. 4a, 4b and 4c illustrate schematic diagrams showing profile modification in shallow trench isolation gap-fill deposition using HARP in the prior art.

Figs. 5a, 5b, 5c, and 5d illustrate schematic diagrams showing effect of the method for removing silicon dioxide on a wafer according to the present invention in the process of profile modification in shallow trench isolation gap-fill deposition using HARP.

Figs. 6a and 6b illustrate schematic diagrams of a device having a native oxide layer and the device after removing the natural oxide layer by the method of the

present invention, respectively.

Figs. 7a and 7b illustrate schematic diagrams of a device having a pad oxide layer and the device after removing the pad oxide layer by the method of the present invention, respectively.

Figs. 8a and 8b illustrate schematic diagrams of a device having a natural oxide layer and the device after removing the natural oxide layer by the method of the present invention, respectively.

Figs. 9a and 9b illustrate schematic diagrams of an integrated circuit device having an oxide recess and the device after removing silicon dioxide by the method of the present invention, respectively.

DETAILED DESCRIPTION

The present invention will be described in further detail below with reference to the accompanying drawings. The accompanying drawings illustrate exemplary implementations of the present invention, but it should be understood that the present invention may be implemented in various forms and should not be limited by the implementations stated herein. Rather, these implementations are provided in order to make the present invention more thorough and complete, and to deliver the scope of the present invention in whole to those skilled in the art.

Fig. 2 illustrates a flow chart of steps of a method for removing silicon dioxide on a wafer according to the present invention.

In this implementation, the method for removing silicon dioxide from a wafer according to the present invention includes: step 201 of introducing dehydrated hydrogen fluoride gas and dehydrated alcohol gas into a process chamber; step 202 of mixing the dehydrated hydrogen fluoride gas and the dehydrated alcohol gas to generate a gaseous etchant; step 203 of causing the etchant to react with substance to be removed, such as silicon dioxide, on a surface of a wafer in the process chamber, and maintaining a high pressure in the process chamber to increase etch selectivity ratio; and step 204 of extracting a reaction product from the process chamber.

The implementation achieves removal of silicon dioxide with high selectivity

ratio and high efficiency, by direct reaction of gaseous etchant with silicon dioxide under the high pressure, and extracting the reaction product after the reaction.

Specific steps of the method for removing silicon dioxide from a wafer according to the present invention are described in detail below.

In one example, substance to be removed on a surface of a wafer is silicon dioxide, and the method for removing silicon dioxide from a wafer according to the present invention may include: step 201 of introducing dehydrated hydrogen fluoride gas and dehydrated alcohol gas into a process chamber; step 202 of mixing the dehydrated hydrogen fluoride gas and the dehydrated alcohol gas to generate a gaseous etchant; step 203 of causing the etchant to react with silicon dioxide on a surface of a wafer in the process chamber, and maintaining a high pressure in the process chamber to increase etch selectivity ratio; and step 204 of extracting a reaction product from the process chamber.

Optionally, conditions for the reaction may include: a pressure in the process chamber is 30Torr to 300Torr, and a temperature in the process chamber is 20°C to 80°C. Further optionally, conditions for the reaction may include: the pressure in the process chamber is 200Torr, and the temperature in the process chamber is 40°C. Experiments have shown that, the higher the pressure in the process chamber within the range of 30Torr to 300Torr, the more readily the gaseous etchant (reactant gas) coagulates at the surface of the wafer and reacts with SiO_2 , in this case, SiO_2 is removed at a significantly increased speed, while Si_3N_4 is removed at a speed which is almost not increased, and as such, remove selectivity ratio (i.e. etch selectivity ratio) of SiO_2 relative to Si_3N_4 (or polycrystalline silicon, HARP deposits, etc.) is enormously increased.

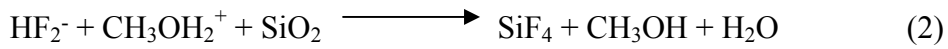
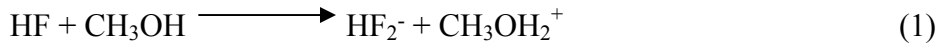
Optionally, a flow rate of the hydrogen fluoride gas may be 100sccm to 500sccm, and a flow rate of the alcohol gas may be 100sccm to 1000sccm. Further preferably, the flow rate of the hydrogen fluoride gas may be 150sccm to 225sccm, and the flow rate of the alcohol gas may be 200sccm to 450sccm.

Optionally, a ratio of the flow rate of the hydrogen fluoride gas to the flow rate of

the alcohol gas may be 0.8:1 to 1.2:1. For example, the ratio of the flow rate of the hydrogen fluoride gas to the flow rate of the alcohol gas may be 0.8:1, 1:1, or 1.2:1. Further preferably, the ratio of the flow rate of the hydrogen fluoride gas to the flow rate of the alcohol gas may be 1:1. By making the flow rate of the hydrogen fluoride gas approach that of the alcohol gas, uniformity of removal of silicon dioxide can be improved.

Optionally, the alcohol gas may be at least one of C₁ to C₈ monohydric alcohol gas. Further preferably, the alcohol gas may be at least one of methanol (CH₃OH), ethanol (C₂H₅OH), and isopropyl alcohol (IPA).

In a case where the alcohol gas is vaporized methanol, the etchant is HF₂⁻ and CH₃OH₂⁺; the reaction product is silicon tetrafluoride, methanol, and water. Specifically, when methanol (CH₃OH) is used, reaction formulae of the method for removing silicon dioxide from a wafer according to the present invention may be as follows:



Dehydrated HF gas and dehydrated CH₃OH gas may be mixed inside the chamber to generate gaseous etchant HF₂⁻ and CH₃OH₂⁺, pressure inside the chamber during the process may be set at 200Torr, temperature inside the chamber may be 40°C, and the mixed HF₂⁻ and CH₃OH₂⁺ react with SiO₂ to produce SiF₄, CH₃OH, and H₂O. CH₃OH has good hygroscopicity, thus can reduce residual H₂O on the wafer surface, and at the same time reaction product such as SiF₄, CH₃OH, and H₂O can all be extracted by a pump after the reaction.

In practical applications, the method for removing silicon dioxide from a wafer according to the present invention may employ a process chamber which may be integrated with a next process into a vacuum platform, as such, the next process may be performed after removing SiO₂ from the wafer surface without destroying a vacuum environment, so as to prevent the wafer from being oxidized again before the

next process because of exposure to non-vacuum environment again, and affecting the next process. The next process, for example, may be NiPt deposition in a silicide process; or SiGe deposition.

The method for removing silicon dioxide from a wafer according to the present invention has the advantages as follows.

Firstly, high selectivity ratio is achieved. The present invention increases the selectivity ratio by high pressure process. Experiments have shown that when employing high pressure process (for example, process pressure of 200Torr), the gaseous etchant coagulates at the surface of the wafer and reacts with SiO_2 more readily, in this case, SiO_2 is removed at a significantly increased speed, while Si_3N_4 is removed at a little increased speed, thereby increasing the remove speed of SiO_2 while reducing damage to the substrate. That is, the method provided by the present invention enormously increases remove selectivity ratio of SiO_2 relative to Si_3N_4 (or polycrystalline silicon, HARP, etc.).

Secondly, no plasma is used, and it is not likely to produce any other by-product, which not only causes no damage to substrate, reduces particle contamination, and keeps clean inside the chamber; but also can cut down apparatus cost.

Thirdly, SiO_2 is removed by chemical reaction, so there is no solid reaction product, and thus the reaction product can be extracted by a pump. Figs. 5a and 5b illustrate schematic diagrams showing another effect of the method for removing silicon dioxide from a wafer according to the present invention. As shown in Fig. 5, since the reaction product diffuses well, removal amount is consistent for SiO_2 in small holes in an intensive area and SiO_2 in a sparse area, the reaction product such as gaseous SiF_4 is easy to be pumped out by a pump, will not block the small hole, thereby achieving good cleaning effect, high cleaning effect for small holes, and high uniformity of removal. Moreover, the method provided by the present embodiment can also improve pad oxide removal and loading effect of shallow trench isolation (STI) recess etching, resulting in consistent deep etching of large and small hole recess, and consistent STI height. Further, CH_3OH and H_2O are also very easy to extract away, will not coagulate on a wall of the chamber, and have few particles.

Fourthly, the method for removing silicon dioxide from a wafer according to an embodiment of the present invention has a low process temperature, for example, 20°C to 80°C, thus high temperature heating is not required, and accordingly, a cooling step corresponding to the high temperature heating step is not required, which means simple reaction process, reaction is completed at one step. As such, not only can process efficiency and capacity be improved, but also can cost produced by at least heating and cooling steps be reduced.

Application Examples

According to another aspect of the present invention, there is also provided a manufacturing method for an integrated circuit, which includes the method for removing silicon dioxide from a wafer described above.

The manufacturing method for an integrated circuit according to the present invention employs the method provided by the above embodiment of the present invention to remove silicon dioxide on a wafer, thus, compared to a manufacturing method for an integrated circuit in the prior art which employs wet etching or plasma dry etching to remove silicon dioxide, the manufacturing method for an integrated circuit according to the present invention can also improve efficiency of removal of silicon dioxide on wafer, reduce damage to substrate, keep cleanness inside the chamber, reduce or even eliminate particle contamination caused by reaction product, and at the same time have characteristics such as simple reaction process, high process efficiency and process capacity, and low cost.

To facilitate understanding of solutions and effects of implementations of the present invention, several application examples are given below. Those skilled in the art should understand that these examples are intended merely to facilitate understanding of the present invention, and no specific details thereof are intended to limit the present invention in any manner.

Example 1: STI HARP deposition gap-fill profile modification:

Figs. 4a, 4b and 4c illustrate schematic diagrams showing profile modification in shallow trench isolation gap fill using HARP (High Aspect Ratio Process) according to the prior art. Fig. 4a shows a device after STI etching, Fig. 4b shows the device during STI HARP deposition, and Fig. 4c shows the device having a void after STI HARP deposition. As shown in Figs. 4a, 4b and 4c, STI HARP deposition is a deposition using CVD method, since a STI aspect ratio of 28nm is high, and STI etching forms a poor profile, it is very likely to generate a void during STI HARP deposition. Furthermore, solid reaction products are produced in the prior art shown in Figs. 4a, 4b, and 4c, cleaning efficiency of small holes is low, and the capacity is low.

The manufacturing method for an integrated circuit in the Example 1 includes a sub-process of profile modification in shallow trench isolate layer gap-fill using HARP. In this sub-process, first, HARP is performed to deposit HARP deposits with a certain thickness using CVD process, then, the method for removing silicon dioxide from a wafer is employed to etch STI to enlarge its opening, and the above-described deposition and etching operations are repeatedly performed until the process ends.

Specifically, Figs. 5a, 5b, 5c, and 5d illustrate schematic diagrams showing effect of the method for removing silicon dioxide from a wafer according to the present invention, in the process of profile modification in shallow trench isolation gap-fill using HARP, Fig. 5a shows a device after STI etching, Fig. 5b shows the device during STI HARP deposition, Fig. 5c shows the device with STI opening modified by the method for removing silicon dioxide from a wafer according to the present invention, and Fig. 5d shows the device after STI HARP deposition.

In this example, the method for removing silicon dioxide from a wafer according to the present invention has the following steps: mixing dehydrated hydrogen fluoride gas and dehydrated methanol to generate gaseous etchant HF_2^- and CH_3OH_2^+ ; then, introducing the etchant into a process chamber such that the etchant contacts and reacts with SiO_2 on a surface of the wafer in the process chamber, producing SiF_4 , CH_3OH , and H_2O . Process conditions inside the process chamber are: a pressure in the chamber is set at 200Torr, a temperature in the chamber is kept at 40°C; after the

reaction is complete, SiF_4 , CH_3OH , and H_2O are pumped out by a pump.

As shown in Figs. 5a, 5b, 5c, and 5d, in the manufacturing method for the integrated circuit provided by the embodiment of the present invention, after HARP is performed using CVD process to deposit HARP deposits with a certain thickness (for example, a SiO_2 layer is deposited), the STI needs to be etched to enlarge the opening, which can avoid the void from being generated. The method of the present invention is used to remove SiO_2 , since a reaction product in non-solid state is easy to be pumped out by a pump, it is possible to keep the chamber clean inside and reduce or even eliminate particle contamination caused by the reaction product. The method provided by the present embodiment requires no high-temperature heating, which means simple reaction process, thereby having characteristics such as high process efficiency and process capacity, and low cost. Further, the method of the present invention has a process pressure of 200Torr and a process temperature of 40°C , thus can increase an etch selectivity ratio of SiO_2 relative to the HARP deposits or the like, which not only improves efficiency of removal of silicon dioxide on wafer, but also reduce damage to substrate, so that the profile of the opening can be controlled, and gap filling capability of CVD HARP can be increased.

Example 2: STI Si_3N_4 natural oxide layer remove:

The manufacturing method for an integrated circuit in this Example 2 includes a sub-process for removing a SiO_2 natural oxide layer on a hard mask layer of the STI, the hard mask layer of the STI is made of Si_3N_4 . In this sub-process, the SiO_2 natural oxide layer on a surface of the hard mask layer of the STI is etched using the method for removing silicon dioxide from a wafer according to the present invention, and etch selectivity ratio of the SiO_2 natural oxide layer relative to the STI HARP deposits is controlled, such that the SiO_2 natural oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is avoided.

Specifically, Figs. 6a and 6b illustrate schematic diagrams of a device having a natural oxide layer and the device after removing the natural oxide layer by the

method of the present invention, respectively.

As shown in Fig. 6a, in the manufacturing method for an integrated circuit, Si_3N_4 is used as the hard mask layer of the STI, and to remove the hard mask layer, it is necessary to use H_3PO_4 wet etching method. However, after a wafer having the hard mask layer is placed in air for a while, a surface of the Si_3N_4 layer will be naturally oxidized to form a compact SiO_2 layer, and the SiO_2 natural oxide layer should be removed before removing Si_3N_4 . If H_3PO_4 wet etching method, which is employed for removing the hard mask layer, is used to remove SiO_2 , SiO_2 will be removed at a very low speed. Furthermore, the STI HARP deposits in Fig. 6a are of a SiO_2 layer deposited using CVD method, the SiO_2 layer has a low compactness, and is easy to remove, in this case, when removing SiO_2 natural oxide layer on the surface of Si_3N_4 layer, it is required to well control removal amount of the STI HARP deposits, that is, to well control an etch selectivity ratio of the SiO_2 natural oxide layer on the surface of Si_3N_4 relative to the STI HARP deposits, to guarantee a step height of the STI (that is, a height of the STI above the surface of the substrate), and because the step height of the STI will affect electric properties of the device, it should be neither too high nor too low.

For this reason, the method of the present invention is necessarily employed to remove the SiO_2 natural oxide layer on the surface of Si_3N_4 , Fig. 6b shows an appearance of a device after removing a SiO_2 natural oxide layer on a surface of Si_3N_4 using the method. In this example, the employed method for removing silicon dioxide according to the present invention has process steps similar to those of Example 1, description of which is omitted herein.

The method of the present invention employs a high-pressure process, which can increase etch selectivity ratio of the SiO_2 natural oxide layer on the surface of Si_3N_4 relative to the STI HARP deposits, so as to rapidly remove the SiO_2 natural oxide layer on the surface of Si_3N_4 , and prevent excessive etching of the STI HARP deposits at the same time, thereby well controlling the step height of the STI; moreover, the method according to the present invention, when removing the SiO_2 natural oxide layer on the surface of Si_3N_4 , does not generate solid reaction product, thus is able to

prevent problem that the reaction product blocks small holes, thereby improving cleaning efficiency of small holes, and improving capacity.

Example 3: IC Pad oxide remove:

The manufacturing method for an integrated circuit in this Example 3 includes a sub-process for removing a pad oxide layer, the pad oxide layer is a SiO_2 layer formed by oxidizing a surface of a substrate by means of heating, which is a buffer layer for a hard mask layer Si_3N_4 of the STI. In this sub-process, the pad oxide layer is etched using the method for removing silicon dioxide from a wafer according to the present invention, and etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits is controlled, such that the pad oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is avoided.

Specifically, Figs. 7a and 7b illustrate schematic diagrams of a device having a pad oxide layer and the device after removing the pad oxide layer by the method of the present invention, respectively.

As shown in Fig. 7a, the pad oxide layer serves as a buffer layer for a hard mask layer Si_3N_4 of the STI, is a SiO_2 layer formed by thermally oxidizing a surface of a substrate using a lamp tube, and its thickness may be determined according to different processes (for example, in 28nm process, the SiO_2 layer has a thickness of 50Å). This SiO_2 pad oxide layer needs to be removed before any subsequent process. Furthermore, the STI HARP deposits in Fig. 7a are of a SiO_2 layer deposited using CVD method, this SiO_2 layer has a low compactness, in this case, when removing the pad oxide layer, it is required to well control removal amount of the STI HARP deposits, that is, to well control an etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits, so that the pad oxide layer can be removed rapidly, while preventing excessive etching of the STI HARP deposits, thereby guaranteeing a step height of the STI.

For this reason, the method of the present invention is necessarily employed to remove the pad oxide layer, and Fig. 7b is a schematic diagram of an appearance of a device after removing the pad oxide layer using the method. In this example, the

employed method for removing silicon dioxide according to the present invention has process steps similar to those of Example 1, description of which is omitted herein.

The method of the present invention employs a high-pressure process, which can increase an etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits, so as to rapidly remove the pad oxide layer, and prevent excessive etching of the STI HARP deposits at the same time, to control a step height of the STI; moreover, the method according to the present invention, when removing pad oxide layer, does not generate solid reaction product, thus is able to improve process efficiency and process capacity, and simultaneously prevent problems such as generation of divot due to wet etching and resultant influence on electric property.

Example 4: natural oxide layer remove before deposition of silicon germanium (SiGe):

The manufacturing method for an integrated circuit in this Example 4 includes a sub-process for removing a SiO₂ natural oxide layer on a silicon substrate before depositing silicon germanium. In this sub-process, the SiO₂ natural oxide layer on the silicon substrate is etched using the method for removing silicon dioxide from a wafer according to the present invention, and an etch selectivity ratio of the SiO₂ natural oxide layer relative to polycrystalline silicon is controlled, such that the SiO₂ natural oxide layer is removed rapidly, and excessive damage to Si substrate is avoided.

Specifically, Figs. 8a and 8b illustrate schematic diagrams of a device having a natural oxide layer and the device after removing the natural oxide layer by the method of the present invention, respectively.

As shown in Fig. 8a, after pre-etching is performed on a Si substrate for a subsequent SiGe deposition, Si substrate in the etching area is exposed to air to be naturally oxidized, the formed natural oxide layer may cause problems such as loss of electric property of the device, therefore, this natural oxide layer needs to be removed completely before depositing SiGe, and Si substrate should not be damaged when removing the SiO₂ layer, that is, an etch selectivity ratio of the SiO₂ natural oxide layer relative to polycrystalline silicon (i.e., Si substrate) needs to be well controlled.

For this reason, the method of the present invention is necessary employed to remove this SiO₂ natural oxide layer, Fig. 8b is a schematic diagram of an appearance of a device after removing the SiO₂ natural oxide layer using the method. In this example, the employed method for removing silicon dioxide according to the present invention has process steps similar to those of Example 1, description of which is omitted herein.

The method of the present invention employs a high-pressure process, which can increase an etch selectivity ratio of SiO₂ natural oxide layer relative to polycrystalline silicon, so as to rapidly remove SiO₂ natural oxide layer, and reduce damage to a gate and the Si substrate at the same time. Moreover, the method according to the present invention, when removing the SiO₂ natural oxide layer, does not generate solid reaction product, thus is able to prevent problems in the prior art that a solid reaction product is produced and the Si substrate suffers from oxidation again during sublimation of the solid reaction product at a high temperature, thus, the manufacturing method for an integrated circuit adopting the method for removing silicon dioxide of the present invention can not only improve process efficiency and process capacity, but also improve performance of the device.

Example 5: natural oxide layer removal before deposition of silicide:

The manufacturing method for an integrated circuit in this Example 5 includes a sub-process for removing a SiO₂ natural oxide layer on a surface of a substrate and a SiO₂ natural oxide layer on a surface of a polycrystalline silicon gate before depositing silicide. In this sub-process, the SiO₂ natural oxide layers on the surface of the substrate and the surface of the polycrystalline silicon gate are etched using the method for removing silicon dioxide from a wafer according to the present invention, and an etch selectivity ratio of the SiO₂ natural oxide layers relative to polycrystalline silicon is controlled, such that the SiO₂ natural oxide layers are removed rapidly, and excessive damage to Si substrate is avoided.

Specifically, Figs. 1a and 3 illustrate schematic diagrams of appearances of a device having a natural oxide layer and the device after removing silicon dioxide by

the method of the present invention, respectively.

As shown in Fig. 1a, when a wafer is placed in air, a surface of Si substrate and a surface of polycrystalline silicon gate will be naturally oxidized to generate compact SiO_2 layers, and in order to avoid excessively large contact resistance between a contact electrode and the substrate, the SiO_2 natural oxide layers need to be removed before depositing Ni or NiPt (5-10%) (which will form NiPt silicide in a subsequent process), but Si substrate should not be damaged in this removing process. Furthermore, at both sides of the polycrystalline silicon gate is Si_3N_4 serving as an insulation spacer, Si_3N_4 should not be damaged either in the process of removing the SiO_2 natural oxide layers.

For this reason, the method of the present invention is necessarily employed to remove this SiO_2 natural oxide layer, Fig. 3 is a schematic diagram of an appearance of a device after removing the SiO_2 natural oxide layer using the method. In this example, the employed method for removing silicon dioxide according to the present invention has process steps similar to those of Example 1, description of which is omitted herein.

The method of the present invention employs a high-pressure process, which can increase an etch selectivity ratio of a SiO_2 natural oxide layer relative to Si_3N_4 and Si substrate, so as to rapidly remove the SiO_2 natural oxide layers on the surface of Si substrate and the surface of polycrystalline silicon gate, and to reduce damage to polycrystalline silicon gate and Si at the same time, preventing problems such as reduction in size of the insulation spacer, increase in electric leakage rate, etc. Moreover, the method according to the present invention, when removing the SiO_2 natural oxide layer, does not generate a solid reaction product, thus is able to prevent problems in the prior art that SiO_2 at a bottom of a hole is inefficiently removed due to the existence of the solid reaction product, and Si substrate suffers from oxidation again during sublimation of the solid reaction product at a high temperature. Thus, the manufacturing method for an integrated circuit using the method for removing silicon dioxide of the present invention can not only improve process efficiency and process capacity, but also improve device performance.

Example 6: STI HARP oxide recess etch:

The manufacturing method for an integrated circuit in this Example 6 includes a STI recess sub-process in a manufacturing method of a 2D NAND memory, the NAND memory includes a floating gate and graphically intensive area STI HARP deposits located in a graphically intensive area, and a control switch gate and graphically sparse area STI HARP deposits located in a graphically sparse area, the floating gate and the control switch gate are made of polycrystalline silicon, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are made of silicon dioxide. In this sub-process, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are etched using the method for removing silicon dioxide from a wafer according to the present invention, and an etch selectivity ratio of the STI HARP deposits relative to the floating gate or relative to the control switch gate is controlled, such that the STI HARP deposits are removed rapidly, and excessive damage to the floating gate and the control switch gate is prevented.

Specifically, Figs. 9a and 9b illustrate schematic diagrams of an integrated circuit device having an oxide recess and the device after removing silicon dioxide by the method of the present invention, respectively.

As shown in Fig. 9a, STI recess process in this example is a process in a manufacturing method of a 2D NAND, NAND is a storage device. In Fig. 9a, the graphically intensive area on the left is a storage area of the device, and includes a floating gate (that is, a deep-colored bar in the graphically intensive area, and made of polycrystalline silicon) and graphically intensive area STI HARP deposits (that is, a light-colored bar in the graphically intensive area and made of silicon dioxide); the graphically sparse area on the right is a control area and includes a source/drain selective control switch gate (that is, a deep-colored bar in the graphically sparse area and made of polycrystalline silicon, simply referred to as “control switch gate” thereafter) and graphically sparse area STI HARP deposits (a light-colored bar in the graphically sparse area and made of silicon dioxide). During STI recess process,

removal amounts of the STI HARP deposits in the graphically intensive area and in the graphically sparse area need to be consistent.

For this reason, the method of the present invention is necessarily employed to remove the STI HARP deposits, and Fig. 9b is a schematic diagram of an appearance of a device after removing silicon dioxide (STI HARP) using the method. In this example, the employed method for removing silicon dioxide according to the present invention has process steps similar to those of Example 1, description of which is omitted herein.

The method of the present invention employs a high-pressure process, which can increase an etch selectivity ratio of the STI HARP deposits relative to the floating gate or relative to the source/drain selective control switch gate, that is, an etch selectivity ratio of SiO_2 relative to polycrystalline silicon, so as to rapidly remove SiO_2 and reduce damage to polycrystalline silicon at the same time. Moreover, the method according to the present invention, when removing SiO_2 , does not generate a solid reaction product, thus is able to prevent problems common in the prior art that a small hole is easily blocked and hardly cleaned because a solid reaction product is produced, and polycrystalline silicon suffers from oxidation again during sublimation of the solid reaction product at a high temperature. Thus, the manufacturing method for an integrated circuit using the method for removing silicon dioxide of the present invention, can not only improve process efficiency and process capacity, but also improve device performance.

Those skilled in the art should understand that the above description of implementations of the present invention only serves the purpose of exemplarily illustrating beneficial effects of implementations of the present invention, and is not intended to limit the implementations of the present invention to any example given.

The foregoing has described implementations of the present invention, the foregoing description is exemplary, not exhaustive, and not limited to the implementations disclosed. Many modifications and variations are apparent for those ordinarily skilled in the art, without departing from the scope and spirit of the

implementations described. Selection of terms used herein, is intended for best explanation of principles of implementations, practical applications or improvement of technology in commercial use, or for enabling others ordinarily skilled in the art to understand implementations disclosed herein.

What is claimed is:

1. A method for removing silicon dioxide from a wafer, comprising:
introducing dehydrated hydrogen fluoride gas and dehydrated alcohol gas into a process chamber;
mixing the dehydrated hydrogen fluoride gas and the dehydrated alcohol gas to generate a gaseous etchant;
causing the etchant to react with a wafer in the process chamber, and maintaining a high pressure in the process chamber to increase an etch selectivity ratio; and
extracting a reaction product from the process chamber.
2. The method for removing silicon dioxide from a wafer according to claim 1, wherein the pressure in the process chamber is in a range of 30Torr to 300Torr.
3. The method for removing silicon dioxide from a wafer according to claim 2, wherein the pressure in the process chamber is 200Torr.
4. The method for removing silicon dioxide from a wafer according to claim 1, wherein a temperature in the process chamber is in a range of 20°C to 80°C.
5. The method for removing silicon dioxide from a wafer according to claim 4, wherein the temperature in the process chamber is 40°C.
6. The method for removing silicon dioxide from a wafer according to claim 1, wherein a flow rate of the hydrogen fluoride gas is in a range of 100sccm to 500sccm, and a flow rate of the alcohol gas is in a range of 100sccm to 1000sccm.
7. The method for removing silicon dioxide from a wafer according to claim 6, wherein the flow rate of the hydrogen fluoride gas is in a range of 150sccm to

225sccm, and the flow rate of the alcohol gas is in a range of 200sccm to 450sccm.

8. The method for removing silicon dioxide from a wafer according to claim 1, wherein a ratio of a flow rate of the hydrogen fluoride gas to a flow rate of the alcohol gas is 0.8:1 to 1.2:1.

9. The method for removing silicon dioxide from a wafer according to claim 6, wherein a ratio of the flow rate of the hydrogen fluoride gas to the flow rate of the alcohol gas is 1:1.

10. The method for removing silicon dioxide from a wafer according to claim 1, wherein the alcohol gas is at least one of C₁ to C₈ monohydric alcohol gas.

11. The method for removing silicon dioxide from a wafer according to claim 10, wherein the alcohol gas is at least one of methanol, ethanol, and isopropyl alcohol.

12. A manufacturing method for an integrated circuit, comprising the method for removing silicon dioxide from a wafer according to any one of claims 1 to 11.

13. The manufacturing method for an integrated circuit according to claim 12, comprising a sub-process of profile modification in a shallow trench isolate layer (STI) gap-fill using a high aspect ratio process (HARP), and

in the sub-process, first, the HARP is performed to deposit STI HARP deposits with a certain thickness using CVD process, then the method for removing silicon dioxide from a wafer is employed to perform an etching operation on the STI to enlarge its opening, and the HARP and the etching operation are repeatedly performed until the manufacturing method ends.

14. The manufacturing method for an integrated circuit according to claim 12, comprising a sub-process for removing a SiO₂ natural oxide layer on a hard mask

layer of the STI, wherein the hard mask layer of the STI is made of Si_3N_4 , and

in the sub-process, the SiO_2 natural oxide layer on a surface of the hard mask layer of the STI is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO_2 natural oxide layer relative to the STI HARP deposits is controlled, such that the SiO_2 natural oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is prevented.

15. The manufacturing method for an integrated circuit according to claim 12, comprising a sub-process for removing a pad oxide layer, wherein the pad oxide layer is a SiO_2 layer formed by oxidizing a surface of a substrate by means of heating, and is a buffer layer for a hard mask layer made of Si_3N_4 of the STI, and

in the sub-process, the pad oxide layer is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the pad oxide layer relative to the STI HARP deposits is controlled, such that the pad oxide layer is removed rapidly, and excessive etching of the STI HARP deposits is prevented.

16. The manufacturing method for an integrated circuit according to claim 12, comprising a sub-process for removing a SiO_2 natural oxide layer on a silicon substrate before depositing silicon germanium, and

in the sub-process, the SiO_2 natural oxide layer on the silicon substrate is etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO_2 natural oxide layer relative to polycrystalline silicon is controlled, such that the SiO_2 natural oxide layer is removed rapidly, and excessive damage to the Si substrate is prevented.

17. The manufacturing method for an integrated circuit according to claim 12, comprising a sub-process for removing a SiO_2 natural oxide layer on a surface of a substrate and a SiO_2 natural oxide layer on a surface of a polycrystalline silicon gate before depositing silicide, and

in the sub-process, the SiO_2 natural oxide layers on the surface of the substrate

and on the surface of the polycrystalline silicon gate are etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the SiO₂ natural oxide layers relative to polycrystalline silicon is controlled, such that the SiO₂ natural oxide layers are removed rapidly, and excessive damage to Si substrate is prevented.

18. The manufacturing method for an integrated circuit according to claim 12, comprising a STI recess sub-process in a manufacturing method of a 2D NAND memory, wherein the NAND memory comprises: a floating gate and graphically intensive area STI HARP deposits located in a graphically intensive area; and a control switch gate and graphically sparse area STI HARP deposits located in a graphically sparse area, the floating gate and the control switch gate are made of polycrystalline silicon, and the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are made of silicon dioxide, and

in the sub-process, the graphically intensive area STI HARP deposits and the graphically sparse area STI HARP deposits are etched using the method for removing silicon dioxide from a wafer, and an etch selectivity ratio of the STI HARP deposits relative to the floating gate or relative to the control switch gate is controlled, such that the STI HARP deposits is removed rapidly, and excessive damage to the floating gate and the control switch gate is prevented.