

METHOD AND SYSTEM FOR MANAGING AN EXPRESS TRAVERSAL OF FLITS IN A NETWORK ON CHIP

ABSTRACT

This document discloses a system and method for managing an express traversal of flits in a network on chip. The system and method disclosed herein manages the allocation of a virtual channel of a downstream processing core/router at an upstream processing core/router. This pre-allocated virtual channel is then subsequently used to receive a packet of data from the upstream processing core/router. Together with the transmission of the flit of data, the downstream router will be informed about the allocation of its virtual channel. Furthermore, each downstream processing core may be configured to bypass an incoming packet of data as required thereby allowing a flit of data to hop across multiple processing cores in a single cycle before the flit of data is buffered.

FIGURE 1