ABSTRACT

A TWO-STEP, LOW ARGON, HDP CVD OXIDE DEPOSITION PROCESS

A method for depositing silicon dioxide between features has been achieved. The method may be applied intermetal dielectrics, interlevel dielectric, or shallow trench isolations. This method prevents dielectric voids, corner clipping, and plasma induced damage in very small feature applications. Features, such as conductive traces, are provided overlying a semiconductor substrate where the spaces between the features form gaps. A silicon dioxide liner layer is deposited overlying the features and lining the gaps, yet leaving the gaps open. The silicon dioxide liner layer depositing step is by high density plasma, chemical vapor deposition (HDP CVD) using a gas mixture comprising silane, oxygen, and argon. The argon gas pressure, chamber pressure, and the sputter rf energy are kept low. A silicon dioxide gap filling layer is deposited overlying the silicon dioxide liner layer to fill the gaps, and the integrated circuit device is completed. The silicon dioxide gap filling layer depositing step is by high density plasma, chemical vapor deposition (HDP CVD) using a gas mixture comprising silane, oxygen, and argon. The argon gas pressure and chamber pressure are kept low while the sputter rf energy is increased.

FIGURE 3 IS SUGGESTED FOR PUBLICATION