

BOOST CONVERTER

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of the filing date of U.S. Provisional Application Ser.
5 No. 60/578,372, filed June 9, 2004, the teachings of which are incorporated herein by reference.

FIELD

This disclosure relates to DC to DC converters, and more particularly to boost DC to DC
converters and controllers for such boost converters.

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BACKGROUND

A DC to DC converter may be used to convert an input DC voltage to an output DC
voltage. A boost converter is a type of DC to DC converter that converts an input DC voltage
into a higher output DC voltage. Such boost converters may be utilized in a variety of electronic
15 devices including portable electronic devices deriving power from a battery source. Usually, the
output voltage is regulated to a required value, while the input voltage varies due to battery
discharging or to variable load current. The output voltage of the boost converter may be
controlled by a controller which controls a state of one or more switches.

One type of control signal provided to the switches may be a pulse width modulated
20 (PWM) signal where the duty cycle of the PWM signal varies to control the state of the switches.
In a boost converter utilizing a PWM control signal the current ripple in an associated inductor of
the boost converter depends on the duty cycle (D) of the PWM control signal. The inductor
current ripple is maximum for $D = 0.5$, and decreases when the duty cycle is either $D > 0.5$ or
 $D < 0.5$. While designing such a boost converter, the worst case inductor current limit should be

taken into consideration. This requires an inductor to support the peak current without saturating the core. For a boost converter controlled by a PWM control signal, the inductor has to be sized for the peak current that occurs at $D = 0.5$, when the input voltage is $V_{IN} = V_{OUT} / 2$. For any other input voltage the peak current will be smaller, thus the inductor will be under utilized. The same under utilization affects all of the boost converter components, including the power switches, and the output and input filtering capacitors meant to smooth the output voltage and filter the input voltage. All these affect negatively the cost, size, and efficiency of the boost converter. Other types of control signals, e.g., pulse frequency modulation (PFM) which varies its frequency, have similar drawbacks as the boost converter controlled by a PWM control signal.

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BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, where like numerals depict like parts, and in which:

15 FIG. 1A is a simplified block diagram of an electronic device having a boost converter consistent with an embodiment;

 FIG. 1B is a block diagram of an embodiment of the boost converter of FIG. 1A;

 FIG. 1C is a timing diagram of the embodiment of FIG. 1B;

 FIG. 1D is another timing diagram of the embodiment of FIG. 1B contrasting operation
20 under heavy and light load conditions;

 FIG. 2A is a block diagram of another embodiment of the boost converter of FIG. 1A;

 FIG. 2B is a timing diagram for the boost converter of FIG. 2A operating in a continuous current mode;

FIG. 2C is a timing diagram for the boost converter of FIG. 2A operating in a discontinuous current mode;

FIG. 3 is a circuit diagram of the voltage controlled current source of FIG. 2A;

FIG. 4 is a circuit diagram of one potential embodiment of the voltage controlled current
5 source of FIG. 3;

FIG. 5 is a circuit diagram of the voltage controlled switch-able current sink of FIG. 2A;

FIG. 6 is a circuit diagram of one potential embodiment of the voltage controlled switch-
able current sink of FIG. 5;

FIG. 7 is a plot of waveforms for V_{cap} , n_{dr} , and p_{dr} of FIG. 2A in a continuous current
10 mode;

FIG. 8 is a plot of waveforms for V_{cap} , n_{dr} , and p_{dr} of FIG. 2A in a discontinuous
current mode;

FIG. 9 is a circuit diagram of one embodiment of the feedback control circuitry of FIG.
2A;

FIG. 10 is a plot of waveforms illustrating voltage and current plots of several
15 components of FIG. 2A; and

FIG. 11 is a circuit diagram of one embodiment of the current sensing circuitry of FIG.
2A.

Although the following Detailed Description will proceed with reference being made to
20 illustrative embodiments, many alternatives, modifications, and variations thereof will be
apparent to those skilled in the art. Accordingly, it is intended that the claimed subject matter be
viewed broadly.

DETAILED DESCRIPTION

FIG. 1A illustrates an electronic device 190 having a boost converter 100 consistent with an embodiment. The electronic device 190 may be any variety of electronic devices, including, but not limited to, a server computer, a desk top computer, a lap top computer, cell phone, personal digital assistant, power tool, etc. The electronic device 190 may receive power from any variety of power sources such as a DC power source 180. The DC power source may be any variety of power sources such as, for example, an AC/DC adapter, a DC "cigarette" type adapter, a battery, or a rechargeable battery. A rechargeable battery may include any type of rechargeable battery such as lithium-ion, nickel-cadmium, nickel-metal hydride batteries, or the like. The boost converter 100 may receive a DC input voltage, V_{in} , and provide an output DC voltage, V_{out} , to a load 170 that is greater than the input voltage V_{in} .

FIG. 1B illustrates a block diagram of one embodiment 100a of the boost converter 100 of FIG. 1 in more detail. In general, the boost converter 100a receives an input DC voltage, V_{IN} , and provides a desired output DC voltage, V_{OUT} greater than V_{IN} . The boost converter 100a may generally include an inductor 112, a main switch SW2 and current sensing circuitry 113, a synchronous switch SW1 109, a rectifying diode 110, and an output capacitor 111. The switch SW1 109 and the current sense circuitry embedded in the circuitry 113 may be omitted in some embodiments. As used herein, "circuitry" may comprise, for example, singly or in any combination, hardwired circuitry, programmable circuitry, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry.

The switch SW2 may be driven ON and OFF by the drivers & break before make (BBM) circuitry 116 via path 115, while the switch SW1 109 may be driven by the same circuitry 116 via path 114. The circuitry 116 may include BBM circuitry to avoid simultaneously conduction

of SW1 and SW2. When the switch SW2 is driven ON, the current through the inductor 112 increases linearly with the slope V_{IN}/L . The amplitude of the current ramp may be proportional to the on-time of SW2. After SW2 is turned OFF, current may be delivered to the output line 103 through the diode 110 or the switch SW1 109. The feedback circuitry 108 may monitor the
5 output voltage V_{OUT} either directly from the output line 103 when the switch SW1 109 is OFF, or from the node 128 when switch SW1 is ON, and provide the comparator 107 with feedback information, e.g., voltage V_{fb} on path 130. This feedback information may embed an output current component beside a voltage one to assure loop stability.

The comparator 107 may compare the feedback voltage V_{fb} on path 130 from the
10 feedback circuitry 108 with the set voltage V_{SET} applied on path 102, and provide the control logic circuitry 121 with a V_{OUT_LOW} signal via path 106 coupled to an output of the comparator 107. The V_{OUT_LOW} signal may therefore be representative of a difference between the output voltage V_{OUT} and the set voltage V_{SET} .

A signal representative of the input voltage V_{IN} may be applied to the voltage controlled
15 t_{ON} generator circuitry 125 via path 124. The voltage controlled t_{ON} generator circuitry 125 may output a pulse having a duration t_{ON} based on the input voltage V_{IN} and a constant. In particular, the t_{ON} duration may be reversely proportional to the input voltage as given by equation (1) where K is the value of the constant.

$$(1) t_{ON} = K / V_{IN}$$

20 In one embodiment, K may be 0.58×10^{-6} . The conversion from V_{IN} to t_{ON} according to equation (1) may be implemented by either analog or by digital means. The t_{ON} pulse may be triggered by the TON_START signal originating from the control logic circuitry 121 via path 122. Control logic circuitry 121 may generate the TON_START signal if the V_{OUT_LOW} signal,

provided by the comparator 107, indicates that the feedback voltage V_{fb} is less than the set voltage V_{SET} . The t_{ON} pulse may be sent to the control logic circuitry 121 via path 123. During the t_{ON} pulse, the control logic circuitry 121 may assert the signal $SW2_ON$ on path 127 to drivers 116. In response, the drivers 116 may drive switch $SW2$ ON. This may then cause an increase of current flowing from V_{IN} through the inductor 112, node 128, and $SW2$. The current slope may be V_{IN}/L during such a condition.

The current ripple in the inductor 112 when $SW2$ is ON may be therefore defined by equation (2).

$$(2) \Delta I_L = (V_{IN}/L) \times t_{ON}$$

The amplitude of the current therefore increases proportionally with t_{ON} and the slope of the rising current. Since t_{ON} is parametrical, as defined in equation (1), equation (2) may be rewritten as detailed in equation (3) substituting in the value of t_{ON} from equation (1) into equation (2).

$$(3) \Delta I_L = (V_{IN}/L) \times (K/V_{IN}) = K/L$$

As can be observed by equation (3), the current ripple ΔI_L is constant because K and L are constants. Advantageously, this feature allows optimal design of the boost converter 100 using in full the current capability of the inductor 112 and the switch $SW2$ in 113. As such, the inductor 112 and other components of the boost converter 100 do not have to be oversized as in a prior art embodiment. Hence, efficiency of the boost converter 100 may be increased. The size of the components may also be decreased to save space in an environment having a premium on such space. The cost of the components may also be less than oversized prior art components.

When t_{ON} has elapsed, the control logic circuitry 121 may switch the $SW2_ON$ signal to non-active. In response, switch $SW2$ may turn off. The control logic circuitry 121 may also

issue the TOFF_START command on path 105 when t_{ON} has elapsed. The TOFF_START command on path 105 may trigger the voltage controlled t_{OFF} generator circuitry 101. The voltage controlled t_{OFF} generator circuitry 101 may output a t_{OFF} pulse via path 129 to the control logic circuitry 121. During t_{OFF} , the control logic circuitry 121 may assert the SW1_ON signal
5 which may then be provided to the drivers 116 via path 126. In response, the drivers 116 may drive switch SW1 119 ON.

The energy accumulated in the inductor 112 may be dissipated during the t_{OFF} time interval to the output line 103, recharging the output capacitor 111 and powering the load (not shown) connected to V_{OUT} . To avoid simultaneous conduction of SW2 and SW1, for a very
10 short time these two switches may be kept OFF by BBM circuitry which may be embedded in the circuitry 116. The current from the inductor 112 may flow during this BBM time interval through the diode 110 to the output line 103.

If the VOUT_LOW signal on path 106 indicates that the feedback voltage V_{fb} is larger than the set voltage V_{SET} when t_{ON} elapses and the TOFF_START signal is generated, the control
15 logic circuitry 121 may keep the TOFF_ACCEL signal inactive. In this case, the duration of the t_{OFF} pulse will correspond to equation (4):

$$(4) t_{OFF} = K / ((V_{SET} * D) - V_{IN}), \text{ where } D \text{ is a feedback factor} = V_{out}/V_{fb}.$$

In contrast, if the signal VOUT_LOW on path 106 indicates that the feedback voltage V_{fb} is less than the set voltage anytime after t_{ON} elapses, the control logic circuitry 121 may
20 make the TOFF_ACCEL signal active. In this case, t_{OFF} will be accelerated, and will have a shorter duration than the one described by equation (4).

When t_{OFF} has elapsed, control logic circuitry 121 may look to the VOUT_LOW signal. If the VOUT_LOW signal on path 106 indicates that the feedback voltage V_{fb} on path 130 is

less than the set voltage V_{SET} , then the control logic circuitry 121 may immediately issue the TON_START command, initiating a new cycle. If the signal VOUT_LOW on path 106 indicates that the output voltage is greater than the set voltage V_{SET} , the control logic circuitry 121 may wait until VOUT_LOW changes state and then issue the TON_START command. In this way, the output voltage V_{OUT} on path 103 may be regulated. This method also provides the advantage of maintaining high efficiency at low load currents by skipping pulses when the load is very small and the capacitor 111 is able to keep the output voltage in the range for a longer time than the switching period.

The current sense circuitry embedded in SW2 & current sense circuitry 113 may protect the power components from over-current conditions. The current sense circuitry may provide via path 117 to the comparator 119 a signal indicative of the inductor current. The current signal on path 117 may then be compared by the comparator 119 with a preset current limit signal OVC_lim from path 118. The output signal from the comparator 118 via path 120 may be active when the inductor current exceeds the preset limit. When the over-current signal on the path 120 is active, the control logic circuitry 121 may de-assert the SW2_ON signal. This may induce the OFF state of the SW2 switch, and trigger the voltage controlled t_{OFF} generator circuitry 101. At the same time, the over-current signal on path 120 may reset the voltage controlled t_{ON} generator circuitry 125. After t_{OFF} elapses, the control logic circuitry 121 may initiate a new cycle by triggering t_{ON} .

Those skilled in the art will recognize that the functions of the above described circuitry 101, 121, 125, 108, 116, and 113 and comparators 107, 119 can be realized using analog circuitry, digital circuitry, or combination of such circuitry. For example, the comparators 107 and 119 should be understood as being either analog or/and digital number comparators.

Similarly, the voltage controlled timing generator circuitry 101 and 125 and the feedback circuitry 108 could be built using analog circuitry as well as using programmable counters, gates, analog to digital converters, etc. Furthermore, the voltage controlled timing generator circuitries 101, 125 and the control logic circuitry 101 may be integrated in a single controller or presenting
5 other partitions as long as the functionality is the same. Nevertheless, the switches and the current sense circuitry may be integrated totally or partially into the same integrated circuit. As used herein, an "integrated circuit" means a semiconductor device and/or microelectronic device, such as, for example, a semiconductor integrated circuit chip.

FIG. 1C is a timing diagram to further detail operation of the embodiment of the boost
10 converter 100a of FIG. 1B. Various input and output signals to the control logic circuitry 101 are illustrated over time. During the time interval between t1 and t2, the voltage controlled t_{ON} generator circuitry 125 may provide a TON_IN pulse of a duration based on the input voltage V_{IN} and the constant K given by equation (1) or $t_{ON} = K / V_{IN}$. In response, the SW2_ON signal may be asserted to turn switch SW2 ON. The inductor current in inductor 112 may begin to
15 ramp up during this time interval between times t1 and t2. The change in inductor current ΔI_L or current ripple during this time interval may be given equation (3) or $\Delta I_L = (V_{IN} / L) \times (K / V_{IN}) = K / L$.

Between times t2 and t3, the voltage controlled t_{OFF} generator circuitry 101 may provide a TOFF_IN pulse equal in length to that detailed in equation (4) or $t_{OFF} = K / ((V_{SET} * D) - V_{IN})$
20 since the VOUT_LOW signal indicates that V_{fb} is greater than V_{SET}. Switch SW1 may be ON and SW2 may be OFF during this time interval and the inductor current may begin to ramp down. At the time t3, the VOUT_LOW signal indicates that V_{fb} is less than V_{SET} hence the TON_START command is immediately issued at this time initiating a new cycle. If V_{fb} is less

than V_{SET} as indicated during the time interval between times t_4 and t_5 , an accelerated T_{off} may occur ($TOFF_ACCEL$ is asserted) where t_{off} may be less than $K / ((V_{SET} * D) - V_{IN})$.

FIG. 1D is a timing diagram to further detail operation of the embodiment of the boost converter 100a of FIG. 1B and contrast operation under heavy and light load conditions.

5 Generally, plot 180 is a plot of inductor current for the inductor 112 over time during light load conditions and plot 182 is a plot of inductor current over time during heavy load conditions. The $VOUT_LOW$ signal provided by comparator 107 may be provide an indication of light and heavy load conditions. When V_{fb} is less than V_{SET} , this may be representative of heavier load conditions and when V_{fb} is greater than V_{SET} , this may be representative of lighter load conditions.

10 conditions.

Between times t_1 and t_2 for plot 180, inductor current may rise during a T_{on} time interval equal to K/V_{in} . Between times t_2 and t_3 for plot 180, inductor current may fall during a t_{off} time interval. The t_{off} time interval between times t_2 and t_3 for plot 180 may be equal to equation (4) or $t_{off} = K / ((V_{SET} * D) - V_{IN})$. At the expiration this time interval at time t_3 , load

15 conditions may still be light load conditions as indicated by the $VOUT_LOW$ signal. At this time t_3 the inductor current may be zero. When the inductor current reaches zero, a reverse current may flow from the higher output voltage source through the high side switch SW1 and inductor 112 into the lower input voltage source V_{in} . To prevent such a reverse current flow, the control logic circuitry 201 opens the high side switch SW1 during the time interval between

20 times t_3 and t_4 of plot 180. The control logic circuitry 201 may keep both switches SW1 and SW2 OFF between times t_3 and t_4 of plot 180 until $VOUT_LOW$ changes states (when $V_{fb} < V_{SET}$) and then start the next T_{ON} cycle at time t_4 . The open state of switches SW1 and SW2 between times t_3 and t_4 of plot 180 may be referred to herein as a skip state. Advantageously

therefore, the control logic circuitry 201 can predict when the zero current inductor condition will be reached (time t3) based on expiration of the time duration defined by equation (4) or $t_{OFF} = K / ((V_{SET} * D) - V_{IN})$.

In contrast, plot 182 illustrates operation under heavier load conditions. Such heavier load conditions may be indicated by the VOUT_LOW signal when Vfb is less than V_{SET} . Between time interval t2 and t3 of plot 182 the t_{OFF} time interval may be less than $K / ((V_{SET} * D) - V_{IN})$. As such, the t_{OFF} period in plot 182 is shortened compared to that of plot 180. At times t3 and t5 of plot 182, the valley of the inductor current of plot 182 is greater than zero and the predictive formulae of a time off interval equal to $K / ((V_{SET} * D) - V_{IN})$ to predict when a zero current inductor condition occurs is not reached in this instance. Hence, a high side and low side switch OFF or skip state is not reached in this instance.

FIG. 2A is a block diagram of another boost converter 100b consistent with another embodiment. The charging current source 1 and discharging current source 2 may generate a voltage waveform at node Vcap, which simulates the current that flows through the inductor L1. The Vcap voltage together with output voltage of the feedback comparator comp3 may trigger the control logic circuitry 201 to generate appropriate pulses to drive the high side switch 204 and low side switch 206.

FIG. 2B is a timing diagram to explain the operation of the boost converter 100b of FIG. 2A operating in a continuous current mode (CCM). Plot fb is a plot representative of the output voltage Vout scaled down by the resistor divider including resistors R2 and R3. The fb plot may be one input to the comparator Comp 3. Plot Vout_1 is plot representative of the output of the comparator Comp3 which compares the fb plot with a reference voltage. This Vout_1 voltage may be provided to the control logic circuitry 201 to inform it whether Vout is less than the

reference voltage. Vcap is a plot representative of the voltage waveform of the internal capacitor C1 which may be input to both comparators Comp1 and Comp2 to control the frequency of the high side switch pdr and low side switch ndr driving signals.

5 The o_detect1 plot may be output from the comparator Comp2 based on a comparison of the Vcap plot and a high threshold level highTH. The o_detect1 plot may send a low signal to the control logic circuitry 201 whenever Vcap goes higher than the highTH. In response, the pdr drive signal that drives the high side switch 204 may go low to drive the high side switch 204 OFF and the low side switch drive signal ndr may go high to drive the low side switch 206 ON. The inductor current of inductor L1 may then begin to ramp up.

10 The o_detect2 plot may be output from the comparator Comp1 based on a comparison of the Vcap plot and a low threshold level lowTH. The o_detect2 plot may send a low signal to the control logic circuitry 201 whenever Vcap goes lower than the lowTH. In response, the pdr drive signal may go high to drive the high side switch 204 ON and the low side switch drive signal ndr may go low to drive the low side switch 206 OFF. The inductor current may then
15 ramp down.

FIG. 2C is another timing diagram to explain the operation of the boost converter 100b of FIG. 2A operating in a discontinuous current mode (DCM). The plots of FIG. 2C represent various inputs and outputs to the comparators Comp1, Comp2, and Comp3, Vcap voltage, high and low side driving signals pdr and ndr, and inductor current flowing in inductor L1 that were
20 detailed with respect to FIG. 2b and any repetitive explanations are omitted herein for clarity. In the DCM of FIG. 2C, the o_detect1 signal again sends a low signal to the control logic circuitry 201 whenever Vcap goes higher than the highTH signal. In response, both the high and low side driving signals pdr and ndr go low in DCM mode.

FIG. 3 illustrates the current source 1 of FIG. 2. This current source may be controlled by the switching signal i_{vin_on} provided to the switch 302 by the control logic circuitry 201. When the switch 302 is open, current source I2 is disconnected from capacitor C1. When the switch 302 is closed, the current source I2 is connected to capacitor C1. Depending, in part, on the position of the switch 502, the capacitor C1 may be charged or discharged.

FIG. 4 is a circuit diagram of one embodiment of the current source of FIG. 3. The voltage divider formed by resistors R6 and R5 may scale down the input voltage V_{in} to a lesser voltage level V_{in_d} where $V_{in_d} = (R5/(R5+R6)) * V_{in}$. The voltage follower formed by opamp 404 and transistor 410 may replicate the V_{in_d} voltage across resistor R4a. This may then result in current I_{R4a} flowing through resistor R4a and transistors 410, 408, and 406. The current mirror formed by transistors 408, 406, 412, and 414 may then mirror current I_{R4a} to switch 302 with a ratio of $(R6+R5)/R5$. The final current flowing through the switch 302 may represent the current level provided by the current source I2 in FIG. 3 given by $I2 = V_{in}/R4a$.

FIG. 5 is a diagram of the discharging current source 2 of FIG. 2. The discharging current source 2 may include a switch 502 and a plurality of current sinks I1, I3, and I4. Current sink I3 may be a current sink proportional to a set voltage, V_{SET} . Current sink I4 may be a current sink of a value greater than I3, e.g., 7 times greater than I3 in one instance. The position of the switch 502 may be responsive to a plurality of control signals from a plurality of sources. The control signals may include the $i1X_on$ signal from the control logic circuitry 201, the $ovcl$ signal output from the comparator Comp4 of the current sensing circuitry 6, and the $vout_1$ signal from the comparator Comp3 of the feedback circuitry 5. The position of the switch 502 may be in switch position 1, 2, 3, or 4 as illustrated in FIG. 2 and 5 depending on the state of the $i1X_on$, $ovcl$, and $vout_1$ signals as detailed in Table 1.

Table 1

ilX_on	vout_1	ovcl	Switch Position
0	X	X	3
1	0	0	1
1	X	1	4
1	1	0	2

5 FIG. 6 depicts one potential embodiment of the switch-able current sink of FIG. 5.

Resistor R4a from FIG. 4 and resistor R4b from FIG. 6 may be matched. The voltage follower
form by opamp 602 and transistor 608 may replicate the Vset voltage across resistor R4b
resulting in current $I_{R4b} = V_{set}/R4b$. Using two set of current mirrors (transistors 604, 606, 610,
612, 614, 616, 618, 620, 622 and 624), I_{R4b} may be mirrored to position 1 and 2 of switch 502.

10 The current levels I_3 and I_4 at position 1 and 2 of switch 502 may be determined by equations
(4a) and (4b).

$$(4a) \ I_3 = I_{R4b} * D$$

$$(4b) \ I_4 = 7 * I_3$$

FIG. 7 illustrates the voltage waveform at the node Vcap, as well as the high side switch
15 204 and low side switch 206 driving pulses when the boost converter of FIG. 2 is operating in a
continuous current mode with reference also to FIGs. 4 and 6. The on time t_{ON} may be
determined by a constant current source with a value equal to $V_{in_d}/R4a$. Whereas, the off time

t_{OFF} may be determined by a constant discharging current source with a value equal to $-(V_{set}-V_{in})/R_{4ab}$. If the value of the capacitor C1 at node Vcap is C and the value of the voltage swing is equal to 1V, one can write, equations (5) and (6).

$$(5) \quad t_{ON} = R_{4a} \times C / V_{in_d}$$

5 (6) $t_{OFF} = R_{4b} \times C / (V_{set}-V_{in_d})$

If $R_{4a} = R_{4b}$, the duty cycle $D = t_{ON} / (t_{ON} + t_{OFF}) = (V_{set}-V_{in_d}) / V_{set}$, which is the well know equation for a boost converter.

FIG. 8 shows the voltage waveform at the node Vcap, as well as the ndr and pdr driving pulses when the converter of FIG. 2 is operating in the discontinuous current mode or pulse skipping mode with reference also to FIGs. 4 and 6. In the discontinuous mode, the high side switch 204 may be turned OFF when the inductor current falls almost to zero to prevent reverse current from the higher output voltage to the lower input voltage. Such a reverse current may not occur under heavier load conditions since the heavy current draw of the load would quickly reduce the output voltage level. Accordingly, the controller for the DC to DC converter is

10 capable of predicting when the inductor current is approaching zero in the discontinuous mode and opening both the high and low side switch to prevent a reverse current flow from the output DC voltage through the high side switch to the input DC voltage during a discontinuous current mode operation of the controller. The controller may predict the inductor current is approaching zero in response to expiration of a time interval based on equation (4).

20 FIG. 9 illustrates the feedback control circuitry 5 of FIG. 2. When the high side switch 204 is turned ON, the switch 902 which may be a single-pole double throw switch may connect the feedback divider 904 including resistors R2, R3 to node LX thereby sensing the output voltage less the voltage drop across the on resistance R_{on} of the high side switch 204. When

high side switch 204 is turned OFF, the switch 902 may connect the feedback divider 904 to Vout. Advantageously, this feedback control may provide a voltage feedback signal summed with an output current component, assuring good loop stability without the need of any current sensing resistor to sense the current level through the inductor L1, which would reduce the converter's efficiency.

FIG. 10 illustrates voltage and current waveforms related with over-current protection. Over-current protection may be achieved by detecting the output current during the on time of the low side switch 206 (e.g., NMOS transistor MN_pow1). If the detected current exceeds a current threshold, the over-current signal (OC) is activated. This may then switch the switch 502 of switch-able current sink to position 4 (Refer to Table 1), and the low side switch 206 may be switched OFF simultaneously with the turning ON of the high side switch 204. In this way, excess current may be discharged through high side switch 204 to the output.

The switch-able sink current 2 with the switch 502 at position 4 may determine the duration of the discharge cycle. This current may be arbitrarily chosen but the value should be less than 1X current sink. At the end of discharge cycle, the inductor current (i.e. the output current) may have dropped below the current threshold. Then normal regulation cycle of the boost converter may resume and current sensing is repeated for subsequent ON cycles of the low side switch 206.

FIG. 11 depicts one embodiment of the current sensing circuitry 6 of FIG. 2. The output current may be sensed using a MOSFET (MN_pow2), which replicates the current flowing through the output NMOS (MN_pow1) or the low side switch when it is ON. Transistor MN_pow2 may have a substantially smaller area ratio with respect to the output NMOS (MN_pow1). By applying the same gate voltage and drain source voltage of MN_pow1 during

its on time to MN_pow2, its current may be proportional to the actual output current of transistor MN_pow1. When transistor MN_pow1 is turned ON, its drain-source voltage may be replicated on the drain-source of transistor MN_pow2 using the switch SW1 and the operational amplifier OPamp1 voltage follower. The gate drive for transistor MN_pow2 may be tied to a fixed
5 voltage that is equal to the gate drive voltage of transistor MN_pow1. The sensed current may be mirrored to resistor R1. The resulting voltage across R1 may then represent the output current.

$$\frac{\text{Area_MN_pow1}}{\text{Area_MN_pow2}} = \frac{\text{Current_in_MN_pow1}}{\text{Current_in_MN_pow2}}$$

By comparing the voltage across R1 with a reference voltage ref2 in the comparator
10 comp4 (see FIG. 2A), the over-current condition may then be detected. When the voltage across resistor R1 exceeds the ref2 voltage, the over-current signal ovcl may be activated. This may then trigger the discharge cycle as described with reference to FIG. 10.

In summary, one embodiment may include a DC to DC converter for converting an input DC voltage to an output DC voltage. The DC to DC converter may comprise at least one switch,
15 an inductor coupled to the at least one switch, and a controller capable of providing a control signal. The at least one switch may be responsive to the control signal in a first state to enter an ON state for an ON time interval, and the ON time interval may be based on the input DC voltage and a constant.

Another embodiment may include an electronic device comprising a DC to DC converter
20 for converting an input DC voltage to an output DC voltage. The DC to DC converter may comprise at least one switch, an inductor coupled to the at least one switch, and a controller capable of providing a control signal. The at least one switch may be responsive to the control

signal in a first state to enter an ON state for an ON time interval, and the ON time interval may be based on the input DC voltage and a constant.

Yet another embodiment may comprise a method. The method may comprise providing a control signal to at least one switch of a DC to DC converter; providing the control signal in a first state, the at least one switch responsive to the control signal in the first state to enter an ON state for an ON time interval; and controlling the ON time interval based on an input DC voltage to the DC to DC converter and a constant.

In yet another embodiment, a boost DC to DC converter for converting an input DC voltage to an output DC voltage higher than the input DC voltage is provided. The boost converter may comprise a high side and low side switch; an inductor coupled to the high and low side switches; and a controller capable of controlling a state of the high and low side switches to switch the high side switch OFF and the low side switch ON during a time ON state. The low side switch may remain ON during the time ON state for an ON time interval based on the input DC voltage and a constant. The controller may further be capable of controlling the state of the high and low side switches to switch the high side switch ON and the low side switch OFF during a time OFF state. The controller may further be capable of predicting when a current level through the inductor reaches zero and controlling the state of the high and low sides switches to switch the high side switch OFF and the low side switch OFF during a skip state to prevent a reverse current flow from the output DC voltage through the high side switch to the input DC voltage.

The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions

thereof), and it is recognized that various modifications are possible within the scope of the claims. Other modifications, variations, and alternatives are also possible. Accordingly, the claims are intended to cover all such equivalents.

What is claimed is:

1. A DC to DC converter for converting an input DC voltage to an output DC voltage,
said DC to DC converter comprising:

at least one switch;

5 an inductor coupled to said at least one switch; and

a controller capable of providing a control signal in a first state, said at least one switch
responsive to said control signal in the first state to enter an ON state for an ON time interval, said
ON time interval based on said input DC voltage and a constant, said controller further capable of
providing said control signal in a second state, said at least one switch responsive to said control
10 signal in the second state to enter an OFF state for an OFF time interval, said OFF time interval
having a length based on a comparison of a signal representative of said output DC voltage with a
set voltage, wherein

said OFF time interval is equal to a value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is greater than said
set voltage, and said OFF time interval is less than said value K of said constant divided by
15 $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is less than
said set voltage, where V_{SET} is a value of said set voltage, D is a feedback factor equal to
said output voltage divided by said signal representative of said output voltage, and V_{IN} is
a value of said input DC voltage.

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2. The DC to DC converter of claim 1, wherein said ON time interval is given by:

$T_{ON} = K/V_{IN}$, wherein T_{ON} is a length of said ON time interval, K is said value of said
constant, and V_{IN} is said value of said input DC voltage.

3. The DC to DC converter of claim 2, wherein a current ripple equal to a value of a change in current level through said inductor during said ON time interval is given by: $\Delta I_L = K/L$, wherein ΔI_L is a value of said current ripple, K is said value of said constant, and L is a value of said inductor.

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4. An electronic device comprising:

a DC to DC converter for converting an input DC voltage to an output DC voltage, said DC to DC converter comprising:

at least one switch;

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an inductor coupled to said at least one switch; and

a controller capable of providing a control signal in a first state, said at least one switch responsive to said control signal in the first state to enter an ON state for an ON time interval, said ON time interval based on said input DC voltage and a constant, said controller further capable of providing said control signal in a second state, said at least one switch responsive to said control signal in the second state to enter an OFF state for an OFF time interval, said OFF time interval having a length based on a comparison of a signal representative of said output DC voltage with a set voltage, wherein

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said OFF time interval is equal to a value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is greater than said set voltage, and said OFF time interval is less than said value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is less than said set voltage, where V_{SET} is a value of said set voltage, D is a feedback factor equal to said output voltage divided by said signal representative of said output voltage, and V_{IN} is a value of said input DC voltage.

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5. The electronic device of claim 4, wherein said ON time interval is given by: $T_{ON} = K/V_{IN}$, wherein T_{ON} is a length of said ON time interval, K is said value of said constant, and V_{IN} is said value of said input DC voltage.

6. The electronic device of claim 5, wherein a current ripple equal to a value of a change in current level through said inductor during said ON time interval is given by: $\Delta I_L = K/L$, wherein ΔI_L is a value of said current ripple, K is said value of said constant, and L is a value of said inductor.

7. A method comprising:

providing a control signal to at least one switch of a DC to DC converter;

providing said control signal in a first state, said at least one switch responsive to said control signal in said first state to enter an ON state for an ON time interval;

controlling said ON time interval based on an input DC voltage to said DC to DC converter and a constant;

providing said control signal in a second state, said at least one switch responsive to said control signal in said second state to enter an OFF state for an OFF time interval;

controlling said OFF time interval based on a comparison of a signal representative of said output DC voltage with a set voltage, which comprises controlling said OFF time interval to be equal to a value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is greater than said set voltage, and controlling said OFF time interval to be less than said value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is less than said set voltage, where V_{SET} is a value of said set voltage, D is a feedback factor equal to said output voltage divided by said signal representative of said output voltage, and V_{IN} is a value of said input DC voltage.

8. The method of claim 7, wherein said ON time interval is given by: $T_{ON} = K/V_{IN}$, wherein T_{ON} is a length of said ON time interval, K is said value of said constant, and V_{IN} is said value of said input DC voltage.

9. The method of claim 8, wherein a current ripple equal to a value of a change in current level through an inductor of said DC to DC converter during said ON time interval is given by: $\Delta I_L = K/L$, wherein ΔI_L is a value of said current ripple, K is said value of said constant, and L is a value of said inductor.

10. The method of claim 9, wherein said at least one switch comprises a low side switch of a boost DC to DC converter.

11. A boost DC to DC converter for converting an input DC voltage to an output DC voltage higher than said input DC voltage, said DC to DC converter comprising:

a high side and low side switch;

an inductor coupled to said high and low side switches; and

a controller capable of controlling a state of said high and low side switches to switch said high side switch OFF and said low side switch ON during a time ON state, said low side switch remaining ON during said time ON state for an ON time interval based on said input DC voltage and a constant, said controller further capable of controlling said state of said high and low side switches to switch said high side switch ON and said low side switch OFF during a time OFF state, said controller further capable of predicting when a current level through said inductor reaches zero and controlling said state of said high and low sides switches to switch said high side switch OFF and said low side switch OFF during a skip state to prevent a reverse current flow from said output DC voltage through said high side switch to said input DC voltage,

wherein OFF time interval has a length based on a comparison of a signal representative of said output DC voltage with a set voltage, said OFF time interval is equal to a value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is greater than said set voltage, and said OFF time interval is less than said value K of said constant divided by $((V_{SET} * D) - V_{IN})$ when said signal representative of said output DC voltage is less than said set voltage, where V_{SET} is a value of said set voltage, D is a feedback factor equal to said output voltage divided by said signal representative of said output voltage, and V_{IN} is a value of said input DC voltage.

12. The boost DC to DC converter of claim 11, wherein said duration of said ON time interval of said low side switch during said first switch state is given by: $T_{ON} = K/V_{IN}$, wherein T_{ON} is a length of said ON time interval, K is said value of said constant, and V_{IN} is said value of said input DC voltage.

13. The boost DC to DC converter of claim 12, wherein a current ripple equal to a value of a change in current level through said inductor during said ON time interval is given by: $\Delta I_L = K/L$, wherein ΔI_L is a value of said current ripple, K is said value of said constant, and L is a value of said inductor.

14. The boost converter of claim 11, wherein said controller predicts said current level through said inductor reaches zero upon expiration of said time OFF state when a duration of said time OFF state is equal to K divided by $((V_{SET} * D) - V_{IN})$, where K is said value of said constant, V_{SET} is a value of a set voltage, D is a feedback factor equal to said output voltage divided by a signal representative of said output voltage, and V_{IN} is said value of said input DC voltage.

15. The boost converter of claim 14, wherein said controller maintains said high and low side switches in said skip state after expiration of said time OFF state until said signal representative of said output voltage becomes less than V_{SET} .

5 16. The boost DC to DC converter of claim 11, further comprising feedback control circuitry capable of sensing a current level through said inductor, said feedback control circuitry comprising a switch and a comparator, said switch coupling said high side switch to an input of said comparator during said time OFF state when said high side switch is ON, said comparator comparing a voltage level based on said output voltage less a voltage drop on said high side
10 switch with a reference voltage level and providing an output signal representative of said current level through said inductor.