CLAIMS

1. A three-dimensional (3D) asynchronous network-on-chip (3D ANOC) architecture, comprising:

a 3D ultra-low power neuromorphic accelerator integrated into the 3D ANOC architecture, the 3D ultra-low power neuromorphic accelerator comprising:

a plurality of tiers;

a global power manager configured to control power for each of the plurality of tiers; and

a plurality of cores defined on each tier and coupled to the global power manager, each core comprising at least:

a local power manager configured to perform snoops on adjacent cores;

a processing element;

a non-volatile memory; and

a communications module.

2. The 3D ANOC architecture of claim 1, in which the local power manager comprises a power management integrated circuit (PMIC).

3. The 3D ANOC architecture of claim 1, in which the non-volatile memory comprises a hybrid distributed memory.

4. The 3D ANOC architecture claim 3, in which the hybrid distributed memory comprises magnetoresistive random access memory (MRAM), resistive random access memory (RRAM), phase-change memory (PCM), or a combination thereof.

5. The 3D ANOC architecture of claim 1, in which each of the plurality of tiers corresponds to a respective layer of a neural network of an edge computing platform.

6. The 3D ANOC architecture of claim 1, in which the communications module communicates with other ones of the plurality of cores on at least one of a same tier, a different tier, or a combination thereof.

7. The 3D ANOC architecture of claim 1, in which the tiers are of a same processing node.

8. A 3D ultra-low power neuromorphic accelerator, comprising:

a plurality of tiers;

a global power manager configured to control power for each of the plurality of tiers; and

a plurality of cores defined on each tier and coupled to the global power manager, each core comprising at least:

a local power manager configured to perform snoops on adjacent cores;

a processing element;

a non-volatile memory; and

a communications module, in which each of the plurality of cores is locally synchronous and globally asynchronous.

9. A 3D ultra-low power neuromorphic accelerator, comprising:

a plurality of tiers;

a global power manager configured to control power for each of the plurality of tiers; and

a plurality of cores defined on each tier and coupled to the global power manager, each core comprising at least:

a local power manager configured to perform snoops on adjacent cores;

a processing element;

a non-volatile memory; and

a communications module, in which the global power manager determines a power state of each of the plurality of cores based on a probabilistic approximation.

10. A 3D ultra-low power neuromorphic accelerator comprising:

a power manager;

a plurality of tiers; and

a plurality of cores defined on each tier and coupled to the power manager, each core comprising at least:

a processing element;

a non-volatile memory; and

a communications module, in which the tiers are of different process nodes.