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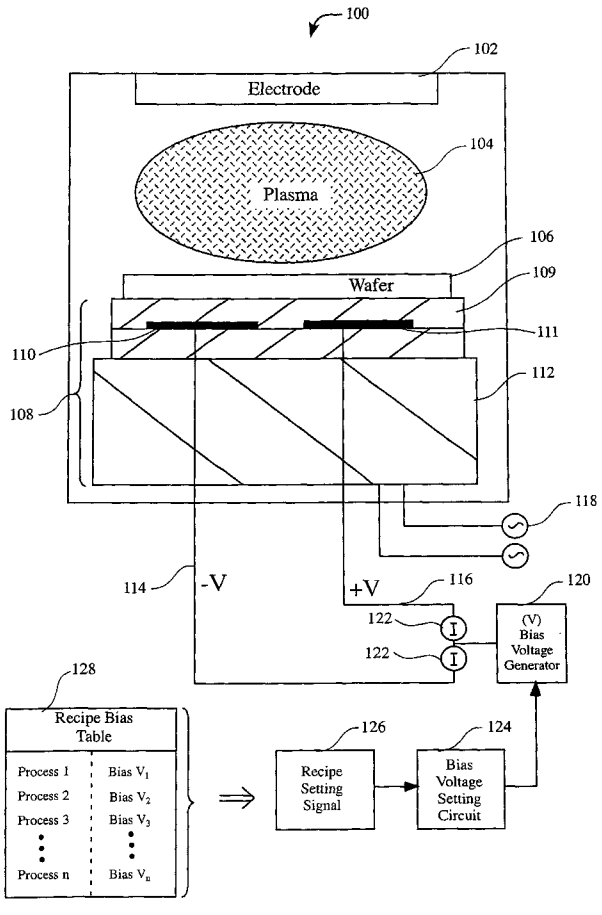
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(54) Title: METHOD FOR REDUCING WAFER ARCING



(57) Abstract: A method for reducing wafer damage during an etching process is provided. In one of the many embodiments, the method includes assigning a bias voltage to each of at least one etching process, and generating the assigned bias voltage before initiation of one of the at least one etching process. The method further includes applying the assigned bias voltage to an electrostatic chuck before initiation of one of the at least one etching processes. The assigned bias voltage level reduces wafer arcing.

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