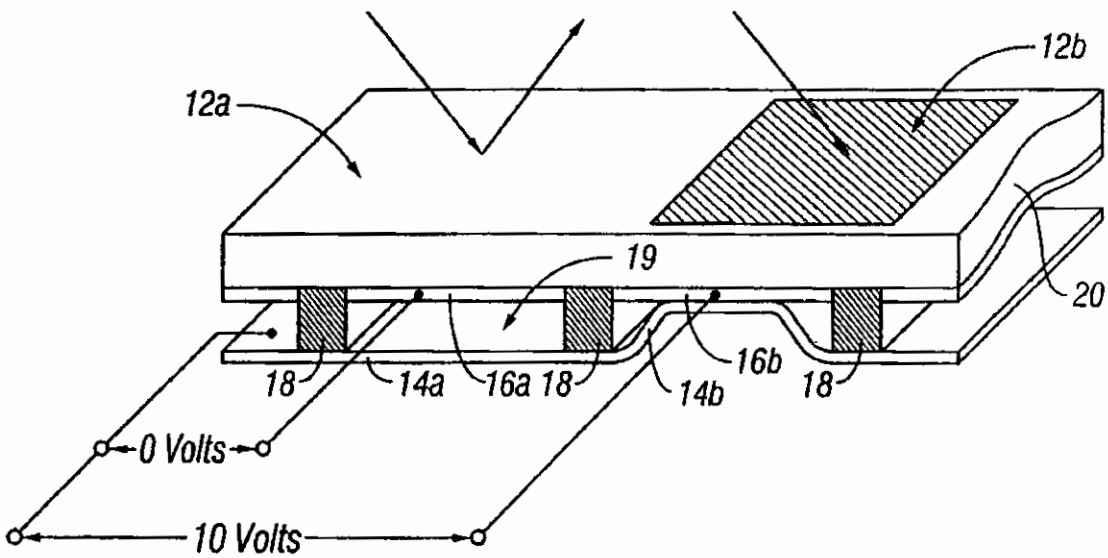

FIG. 1

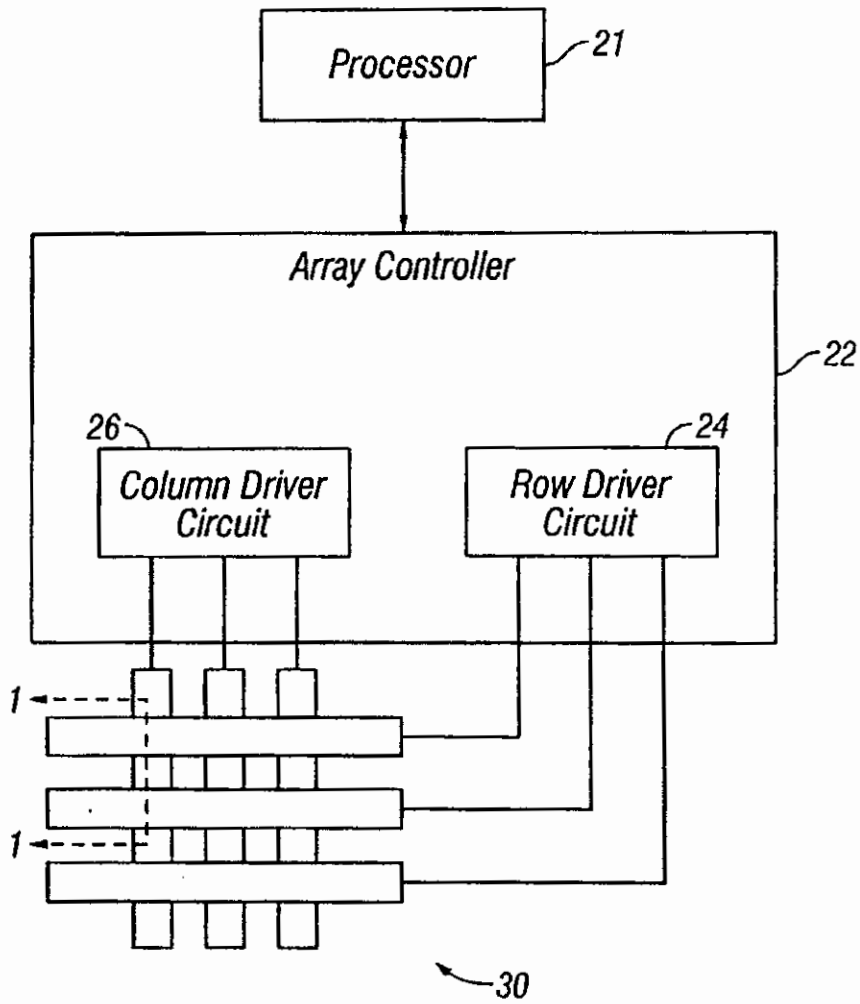
Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

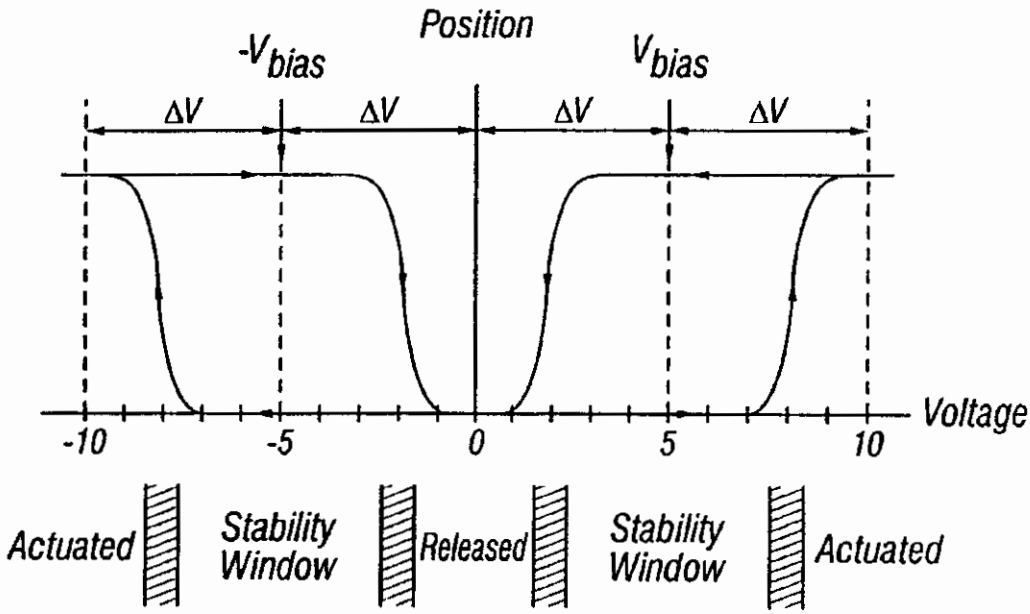

FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate
$-\Delta V$	Actuate	Release

FIG. 4

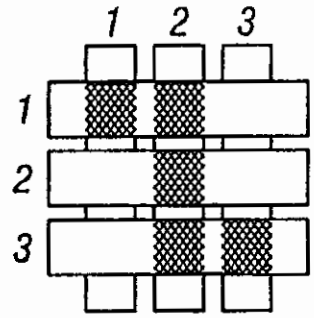
1
2
3
1
2
3

FIG. 5A

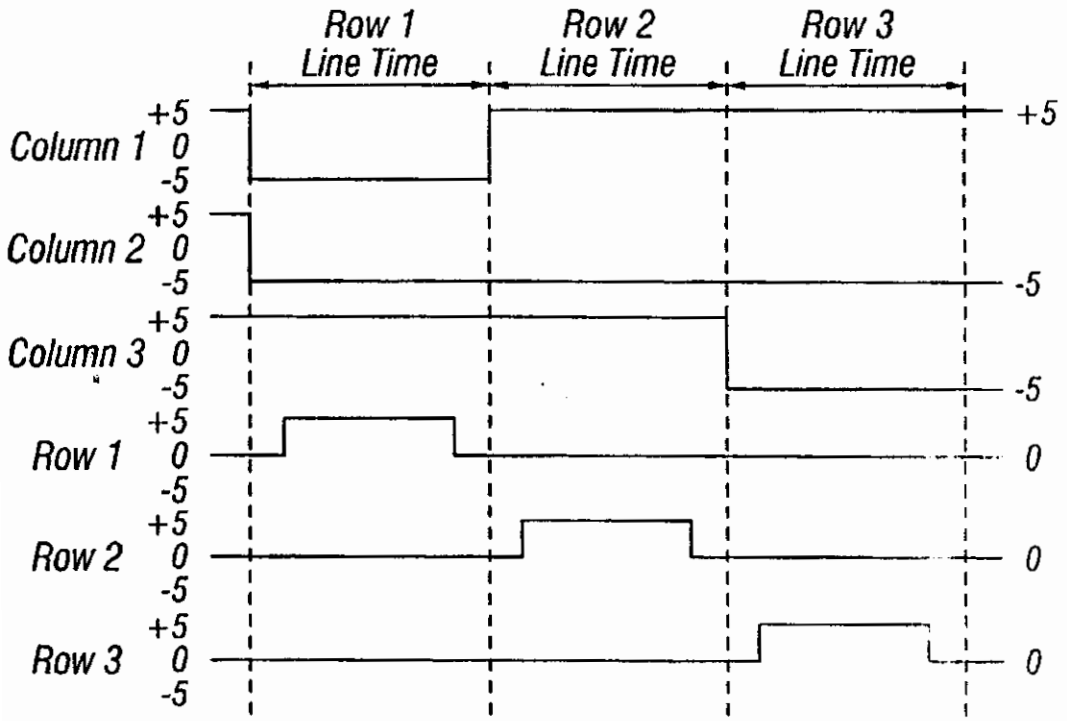
Row 1
Line Time
Row 2
Line Time
Row 3
Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

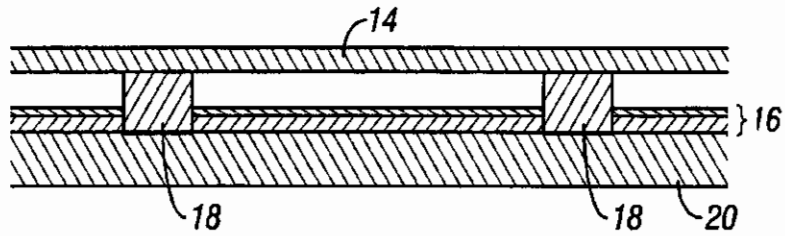

FIG. 6A

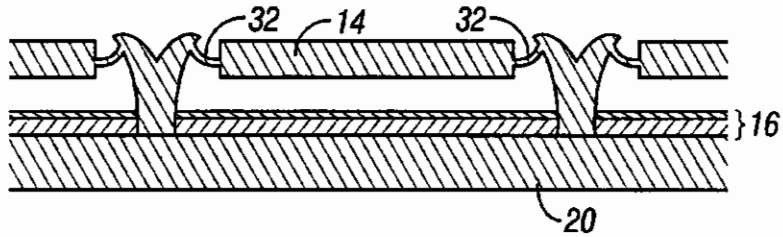

FIG. 6B

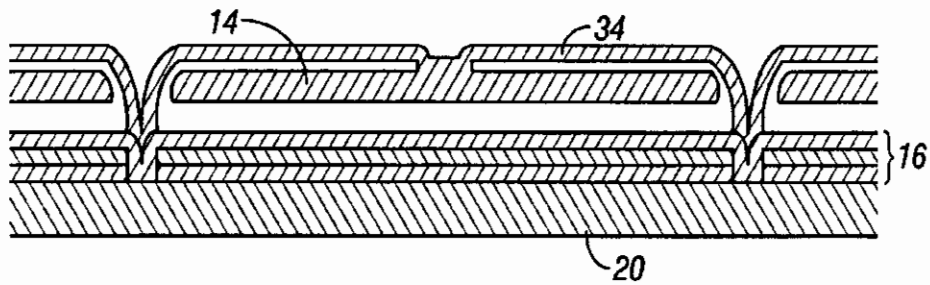

FIG. 6C

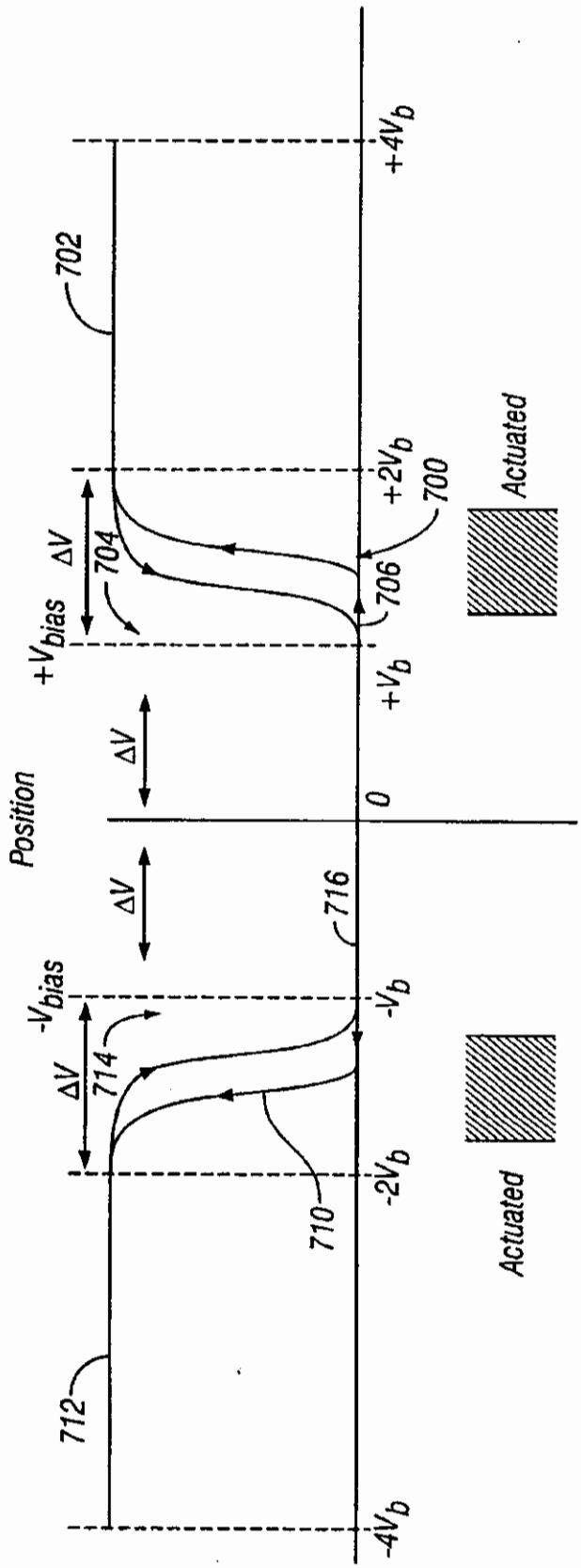
+4Vb
+2Vb
+Vb
0
-Vb
-2Vb
-4Vb
+Vbias
-Vbias
ΔV
Position
Released
Actuated
Actuated
700
702
704
706
710
712
714
716

FIG. 7

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Slowly Releasing (V_b)	Slowly Releasing ($-V_b$)
$+\Delta V$	Release (0)	Actuate ($-2V_b$)
$-\Delta V$	Actuate ($2V_b$)	Release (0)

FIG. 8

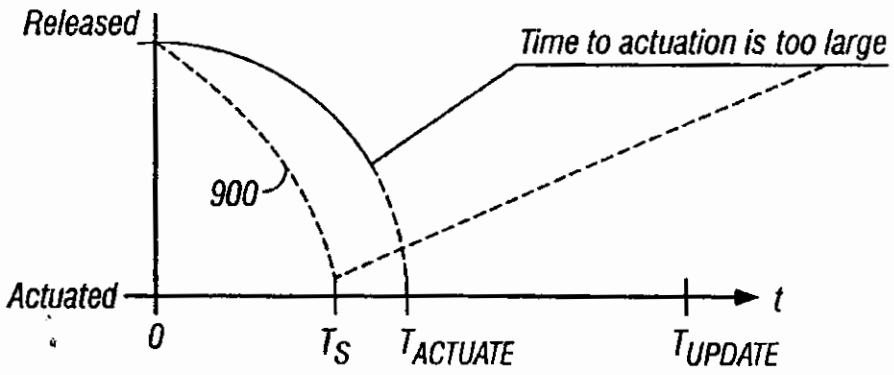

FIG. 9

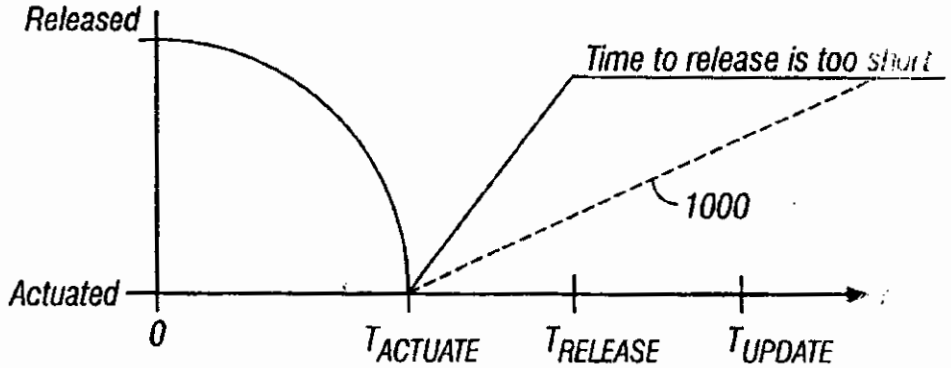

FIG. 10

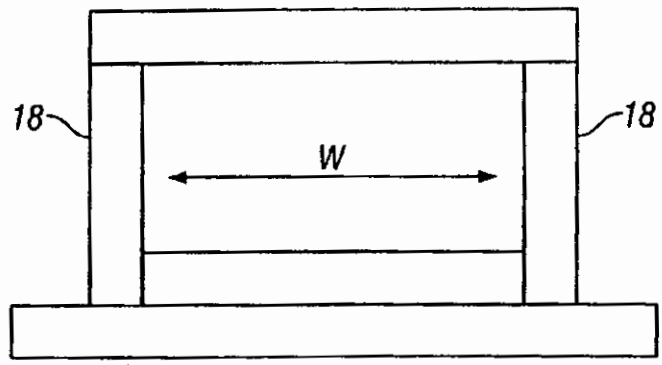

FIG. 11A

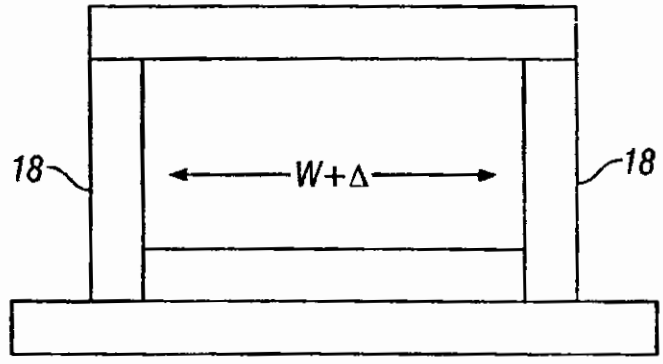

FIG. 11B

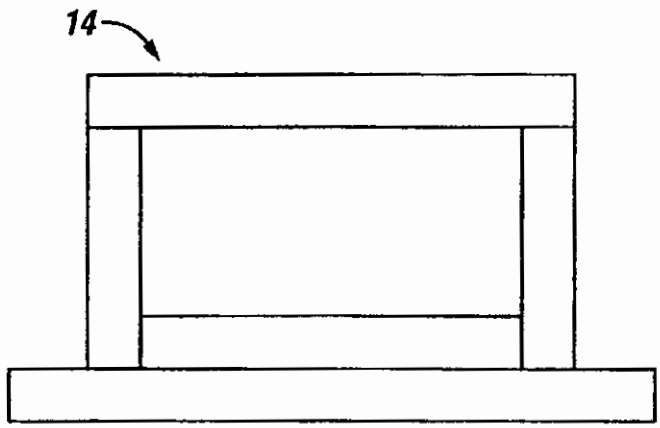

FIG. 12A

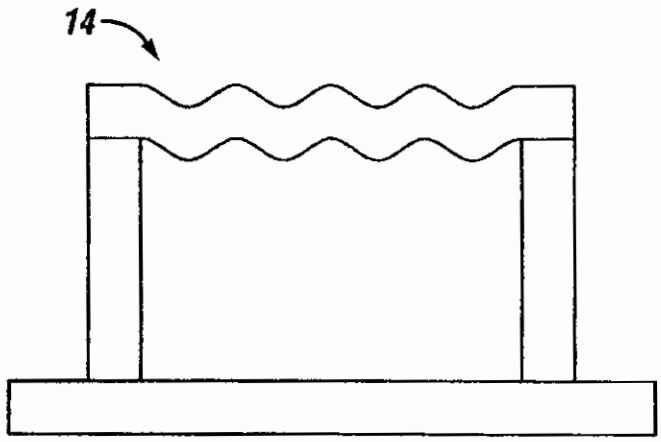

FIG. 12B

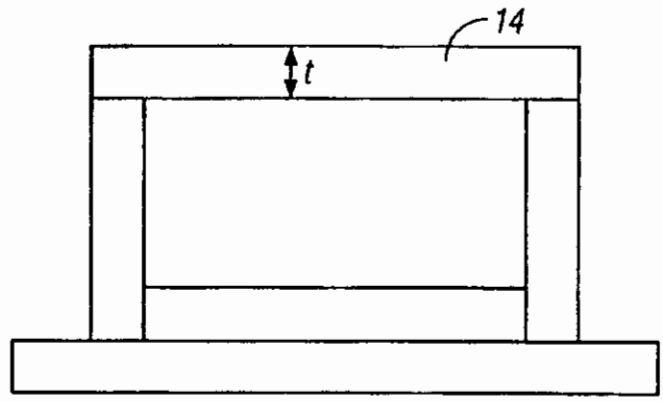

FIG. 13A

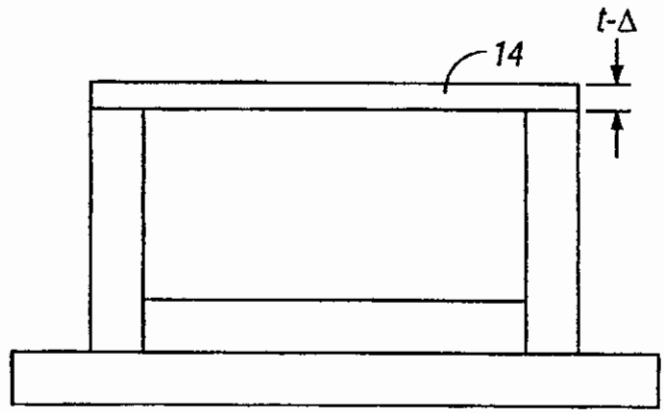

FIG. 13B

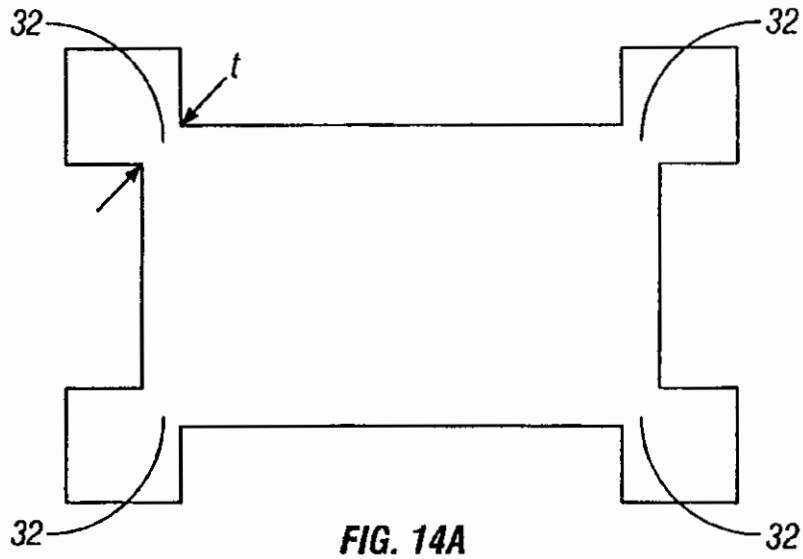

FIG. 14A

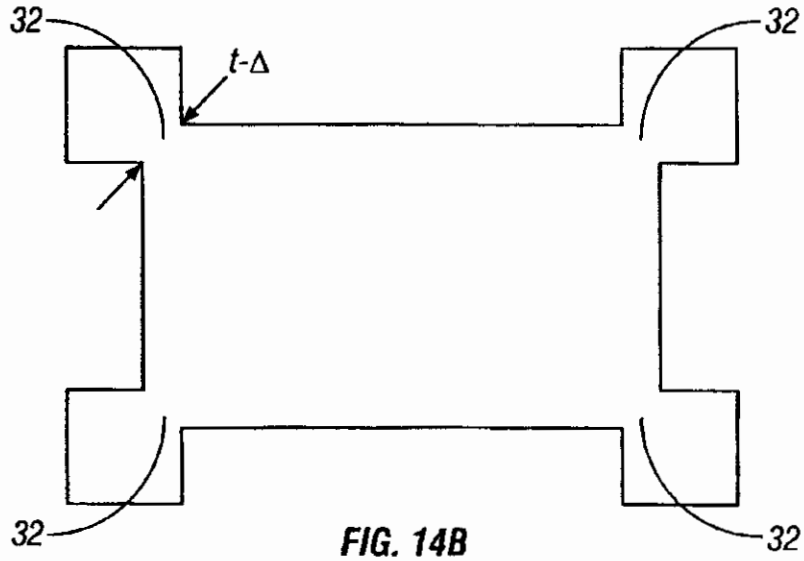

FIG. 14B

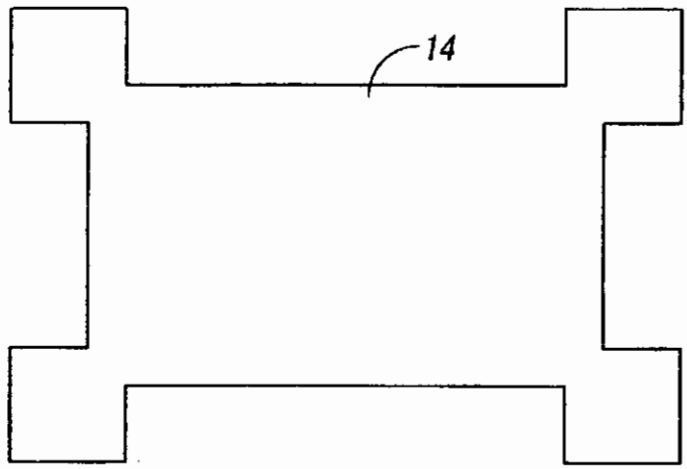

FIG. 15A

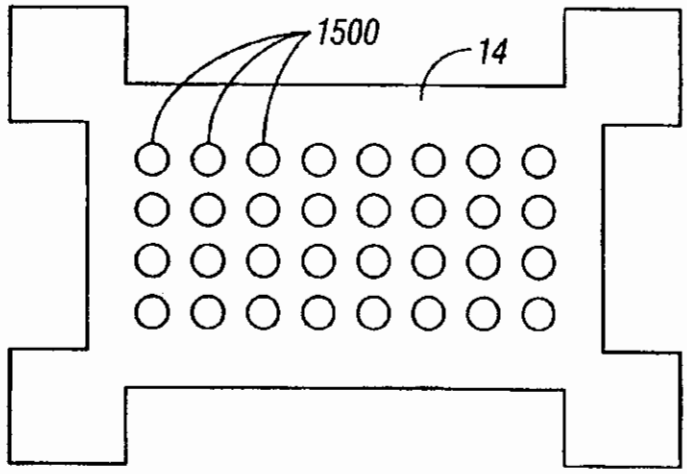

FIG. 15B

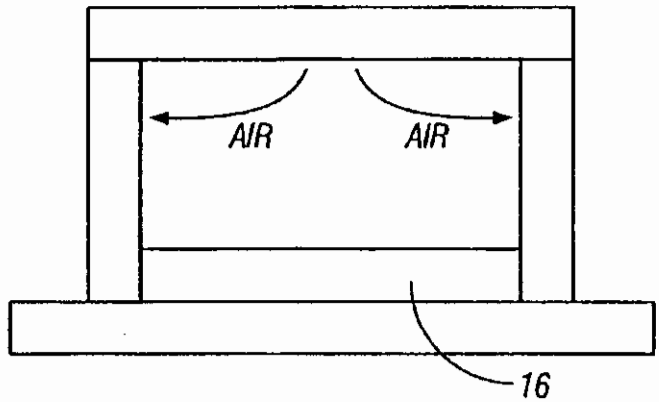

FIG. 16A

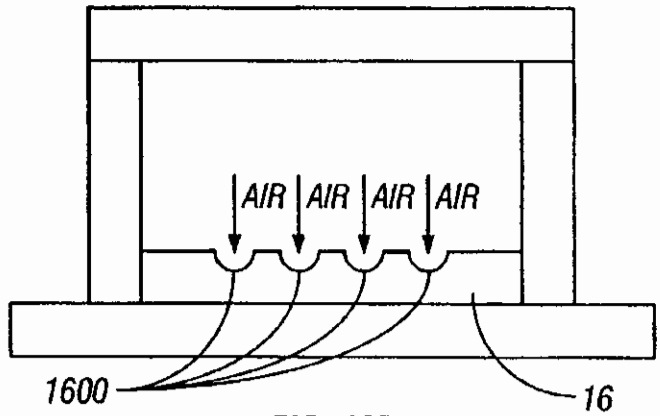

FIG. 16B

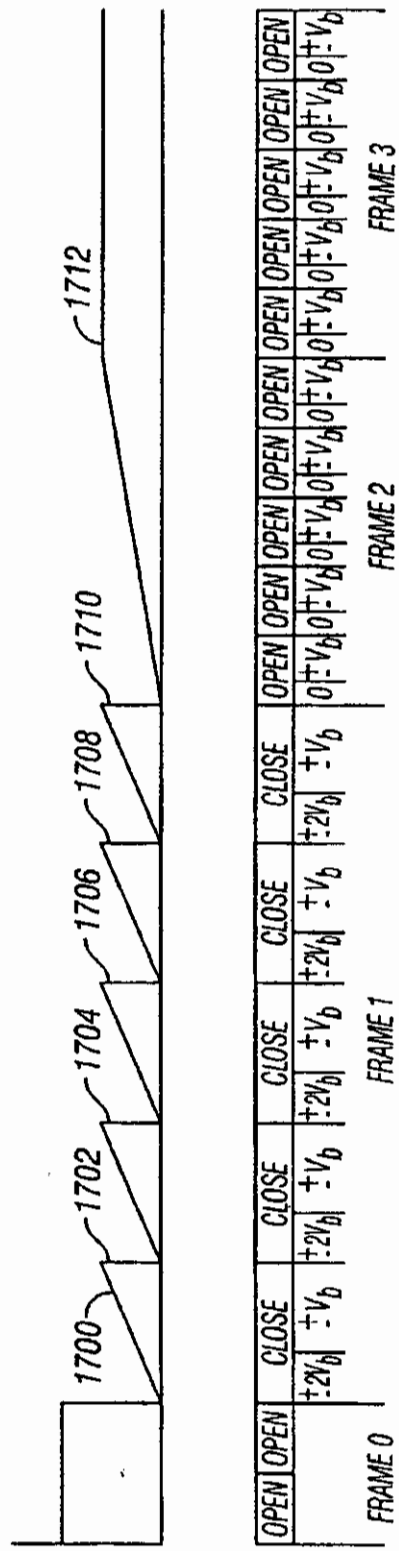
RELEASED
ACTUATED
1700
1702
1704
1706
1708
1710
1712
OPEN
CLOSE
±2Vb
±Vb
0
FRAME 0
FRAME 1
FRAME 2
FRAME 3

FIG. 17

	Column Output Signals	
	$+2V_{bias}$	$-2V_{bias}$
0	Slowly Actuating ($+2V_b$)	Slowly Actuating ($-2V_b$)
$+2\Delta V$	Release (0)	Actuate ($-4V_b$)
$-2\Delta V$	Actuate ($+4V_b$)	Release (0)

FIG. 18

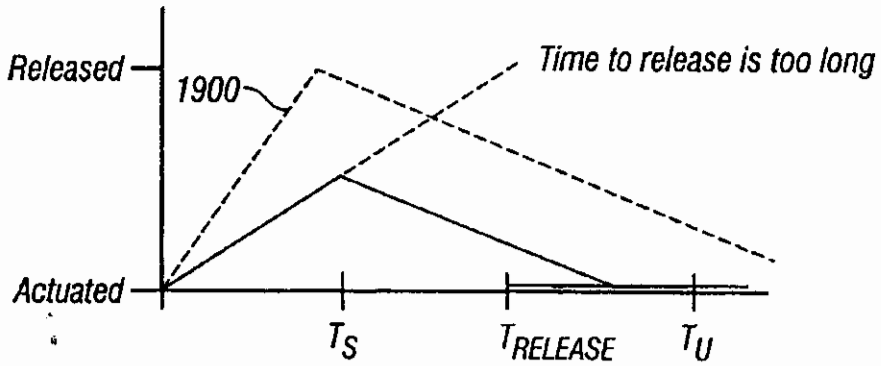

FIG. 19

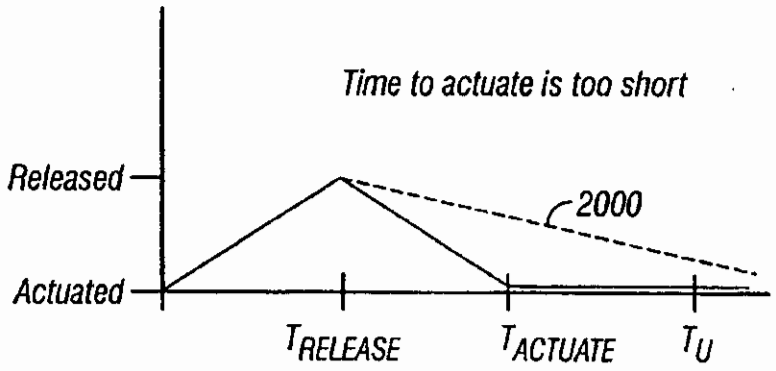

FIG. 20

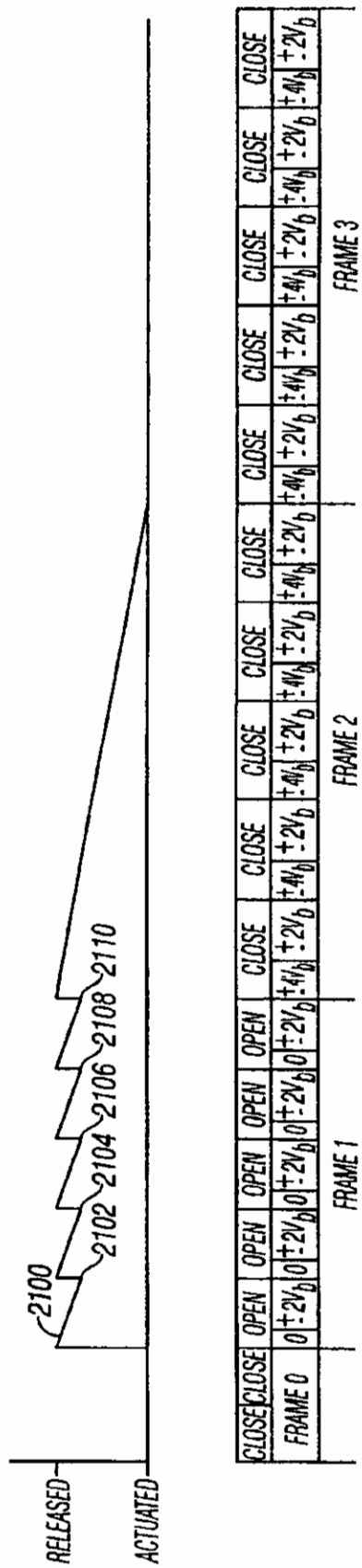
RELEASED
ACTUATED
2100
2102
2104
2106
2108
2110
CLOSE CLOSE OPEN OPEN OPEN OPEN CLOSE CLOSE CLOSE CLOSE CLOSE CLOSE CLOSE CLOSE CLOSE CLOSE
FRAME 0
FRAME 1
FRAME 2
FRAME 3

FIG. 21

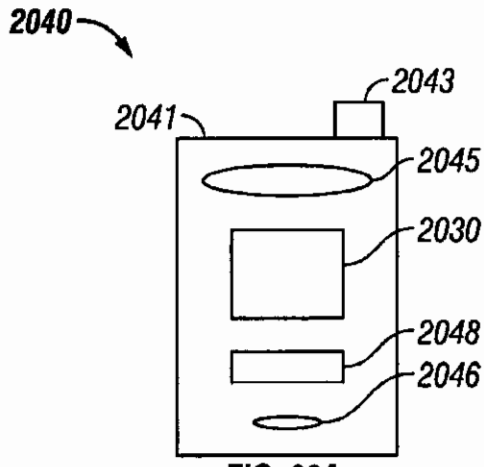

FIG. 22A

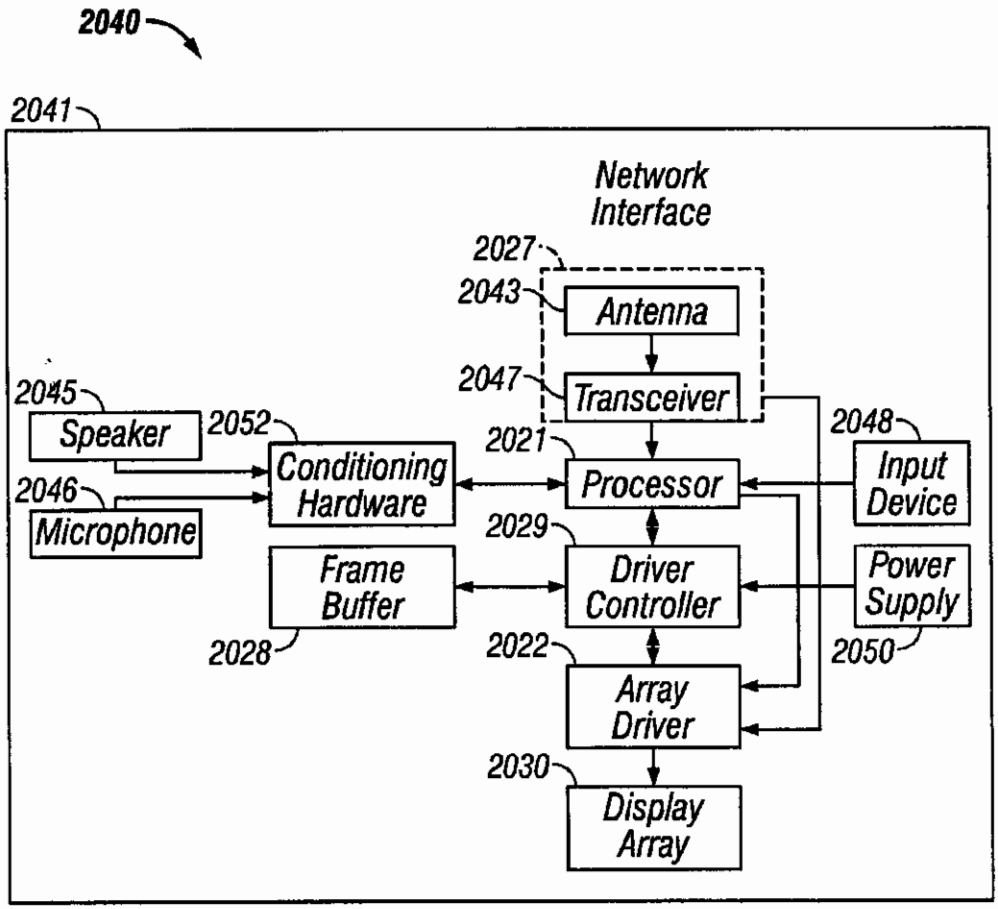

FIG. 22B