STRUCTURE AND METHOD FOR FINFET INTEGRATED WITH CAPACITOR

ABSTRACT

The present disclosure provides one embodiment of a semiconductor structure that includes a semiconductor substrate having a first region and a second region; a shallow trench isolation (STI) feature formed in the semiconductor substrate. The STI feature includes a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and having a second thickness T2 greater than the first depth, the first portion of the STI feature being recessed from the second portion of the STI feature. The semiconductor structure also includes a plurality of fin active regions on the semiconductor substrate; and a plurality of conductive features disposed on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region.

Figure 2