A FLASH MEMORY CELL AND ITS METHOD OF FABRICATION

ABSTRACT OF THE DISCLOSURE

A flash memory EEPROM transistor is formed on a surface of a semiconductor substrate. In portions of the substrate, at the surface thereof, a doped source region and a doped drain region are formed with a channel region therebetween. A tunnel silicon oxide dielectric layer is formed over the semiconductor substrate aside from the source region. Above the source region is formed a gate oxide layer which is thicker than the tunnel oxide layer. Above a portion of the tunnel oxide dielectric layer, over the channel region and above a portion of the gate oxide layer is formed a stacked-gate structure for the transistor comprising a floating gate layer, an interelectrode dielectric layer, and a control gate layer. The source region is located on one side of the stacked gate structure with one edge of the source region overlapping the gate structure. The drain region which is located on the other side of the stacked gate structure with one edge thereof overlapping the gate structure.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)