~~What is claimed is:~~Claims

1. A device, comprising:

a cis well associated with a cis electrode;

a trans well associated with a trans electrode;

a field effect transistor (FET) positioned between the cis well and the trans well, the field effect transistor (FET) including:

a fluidic system defined therein, the fluidic system including:

a first cavity facing the cis well;

a second cavity fluidically connected to the trans well; and

a through via extending through the field effect transistor from the first cavity;

a first nanoscale opening fluidically connecting the cis well and the first cavity, the first nanoscale opening having an inner diameter; and

a second nanoscale opening fluidically connecting the through via and the second cavity, the second nanoscale opening having an inner diameter, wherein the second nanoscale opening inner diameter is larger than the first nanoscale opening inner diameter.

2. The device as defined in claim 1, wherein:

the second nanoscale opening inner diameter is at least ~~about~~ two times larger than the first nanoscale opening inner diameter;

the first nanoscale opening inner diameter ranges from about 1 nm to about 3 nm; and

the second nanoscale opening inner diameter ranges from about 2 nm to about 20 nm.

3. The device as defined in claim 1, wherein the second nanoscale opening inner diameter ranges from about two times larger than the first nanoscale opening inner diameter to about five times larger than the first nanoscale opening inner diameter.

4. The device as defined in claim 1, wherein:

the first nanoscale opening inner diameter ranges from about 0.5 nm to about 3 nm; and

the second nanoscale opening inner diameter ranges from about 10 nm to about 20 nm.

5. The device as defined in claim 1, wherein:

the second nanoscale opening inner diameter is about three times larger than the first nanoscale opening inner diameter;

the first nanoscale opening inner diameter ranges from about 1 nm to about 2 nm; and

the second nanoscale opening inner diameter ranges from about 10 nm to about 20 nm.

6. The device as defined in any of claims 1 through 5, further comprising a membrane positioned between the cis well and the first cavity, wherein the first nanoscale opening extends through the membrane.

7. The device as defined in claim 6, wherein the membrane is selected from the group consisting of a lipid and a biomimetic equivalent of a lipid.

8. The device as defined in claim 7 wherein the first nanoscale opening extends through: a polynucleotide nanopore; a polypeptide nanopore; or a carbon nanotube, disposed in the membrane.

9. The device as defined in claim 6, wherein the membrane is a synthetic membrane, and wherein the first nanoscale opening is a solid state nanopore.

10. The device as defined in any of claims 1 through 9, wherein:

the first nanoscale opening has a variable electrical resistance; and

the second nanoscale opening has ~~an at least~~ a substantially fixed electrical resistance.

11. The device as defined in any of claims 1 through 10, wherein the device comprises a nanopore sequencer.

12. An array of a plurality of the ~~nanopore sequencers~~ devices as defined in claim 11, wherein:

each of the plurality of the ~~nanopore sequencers~~ devices shares a common cis electrode and a common trans electrode; or

each of the plurality of the ~~nanopore sequencers~~ devices has a distinct cis electrode and a distinct trans electrode; or

each of the plurality of the ~~nanopore sequencers~~ devices shares a common cis electrode and has a distinct trans electrode; or

each of the plurality of the ~~nanopore sequencers~~ devices has a distinct cis electrode and shares a common trans electrode.

13. A method of using the device as defined in any of claims 1 through ~~12~~11, the method comprising:

introducing an electrolyte into each of the cis well, the trans well, the first cavity, the FET through via, and the second cavity;

applying a voltage bias between the cis electrode and the trans electrode sufficient to drive a polynucleotide through the first nanoscale opening, wherein an electrical resistance of the first nanoscale opening varies in response to an identity of bases in the polynucleotide, and wherein a potential of the electrolyte in the FET through via varies in response to the variation in electrical resistance of the first nanoscale opening; and

measuring a response of the FET as the polynucleotide is driven through the first nanoscale opening, to identify the bases in the polynucleotide.

14. The method as defined in claim 13, wherein the FET further comprises a source, a drain, and a channel, and wherein measuring the response of the FET includes:

measuring a source-drain current; or

measuring a potential at the source, the drain, or both the source and the drain; or

measuring a resistance of the channel; or

combinations thereof.

15. A method, comprising:

fabricating a field effect transistor;

defining a fluidic system therein, the fluidic system including:

a first cavity having an inlet end and an outlet end; and

a second cavity opposed to the first cavity;

defining a through via through the field effect transistor from the first cavity outlet end toward the second cavity;

defining a membrane over the inlet end of the first cavity, the membrane having a first nanoscale opening therethrough, the first nanoscale opening having an inner diameter; and

defining a second nanoscale opening through a base substrate of the field effect transistor to fluidically connect the through via with the second cavity, the second nanoscale opening having an inner diameter, wherein the second nanoscale opening inner diameter is larger than the first nanoscale opening inner diameter.

16. The method as defined in claim 15, further comprising:

fluidically connecting a cis well to the first nanoscale opening, the cis well being associated with a cis electrode;

fluidically connecting a trans well to the second cavity, the trans well being associated with a trans electrode, thereby forming a nanopore sequencer; and

immersing the nanopore sequencer into an electrolyte.

17. The method as defined in claim 15, wherein fabricating the field effect transistor comprises:

defining a source, a drain, and a channel in a silicon layer of a silicon on insulator substrate;

oxidizing a surface of the silicon layer to form a gate oxide on the source, the drain, and the channel;

forming a sacrificial layer on the gate oxide on the channel;

depositing an etch stop material to form a layer on the gate oxide on the source and on the drain and on the sacrificial layer and to form the base substrate; and

fabricating a vertical interconnect access (via) and a metallic interconnect partially encapsulated in an insulating material, the via electrically connecting the source and drain to the metallic interconnects.

18. The method as defined in claim 17, wherein prior to depositing the etch stop material, the method further comprises defining the second cavity of the fluidic system by etching a portion of ~~the~~ a second silicon layer through to an insulator layer of the silicon on insulator substrate, wherein the portion etched away is opposed to the channel.

19. The method as defined in claim 18, wherein the etch stop material is a solid state material that is deposited on the second silicon layer and an exposed portion of the insulator layer to form the base substrate.

20. The method as defined in claim 19, wherein the second nanoscale opening is defined by etching through a portion of the solid state material.

21. The method as defined in claims 19 or 20, wherein:

defining the first cavity comprises:

etching an area of the insulating material through to the sacrificial layer, wherein the area abuts the channel; and

etching the sacrificial layer to expose the gate oxide on the channel; and

defining the through via comprises etching through respective portions of each of the gate oxide, the silicon layer of the silicon on insulator substrate, and the insulating layer of the silicon on insulator substrate to expose the solid state material.

22. The method as defined in claim 21, further comprising oxidizing exposed portions of the silicon layer of the silicon on insulator substrate in the through via.

23. The method as defined in claim 21, further comprising depositing or growing an insulating layer on exposed portions of the silicon layer of the silicon on insulator substrate in the through via.