

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
17 June 2021 (17.06.2021)



(10) International Publication Number
WO 2021/116795 A1

(51) International Patent Classification:
H03H 11/24 (2006.01)

(21) International Application Number:
PCT/IB2020/060645

(22) International Filing Date:
12 November 2020 (12.11.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2024412 10 December 2019 (10.12.2019) NL

(71) Applicant: **INSIAVA (PTY) LTD.** [ZA/ZA]; Atterbury
Estate, Building 7, First Floor, 19 Frikkie de Beer Street,
0063 Pretoria (ZA).

(72) Inventors: **SUNTKEN, Artur, Wilhelm**; Plot 146 Luiperd
Road, Tierpoort, 0056 Pretoria (ZA). **FAURÉ, Nicolaas,
Mattheus**; 816 Darling Street, Waverley, 0186 Pretoria
(ZA).

(74) Agent: **DAVIES, James, Hasely**; Adams & Adams, PO
Box 1014, 0001 Pretoria (ZA).

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN,
KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO,
NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW,

(54) Title: AN ELECTRONIC CIRCUIT THAT GENERATES A HIGH-IMPEDANCE LOAD AND AN ASSOCIATED METHOD

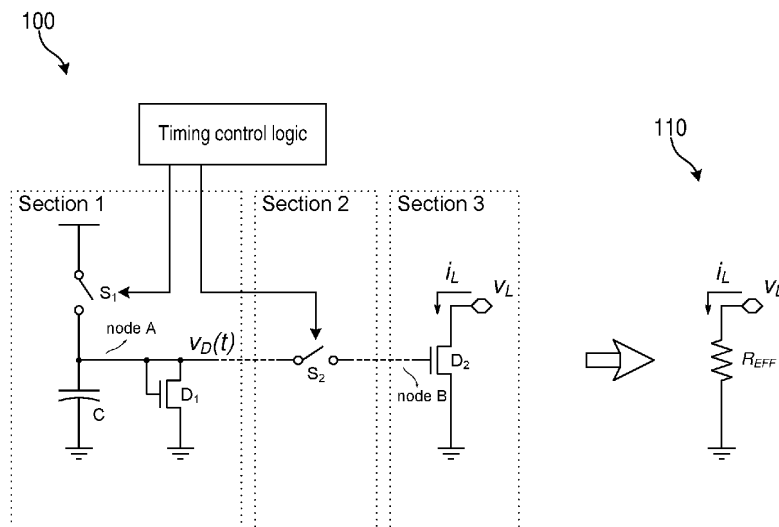


FIG. 3

(57) Abstract: An electronic circuit configured to present a high-impedance load between a load point (V_L) and a reference point includes a capacitive element (C) provided between a first node (Node A) and the reference point, a first element (D_1) connected in parallel with the capacitive element (C), a first switching element (S_1) provided in series between the first node (A) and a voltage source point, a second switching element (S_2) provided between the first node (A) and a second node (Node B), a second element (D_2) connected between the second switching element (S_2), the load point, and the reference point, and timing control logic configured to implement three stages. In a charging stage, the first switching element (S_1) is closed and the second switching element (S_2) to charge a nodal voltage $v_D(t)$ at the first node (A). In discharge stage, the first switching element (S_1) is open and the second switching element (S_2) is closed to discharge the nodal voltage $v_D(t)$ at the first node (A).

[Continued on next page]

WO 2021/116795 A1

SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to the identity of the inventor (Rule 4.17(i))*
- *of inventorship (Rule 4.17(iv))*

Published:

- *with international search report (Art. 21(3))*
- *with amended claims (Art. 19(1))*
- *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*

is open and the second switching element (S_2) is open to enable discharging of the capacitive element (C) through the first element (D_1). In a transfer stage, the second switching element (S_2) is closed to connect the first node (A) and the second node (B), after which the second switching element (S_2) is opened and the second element (D_2) is biased to present the high-impedance load.