$$H = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

FIG. 1

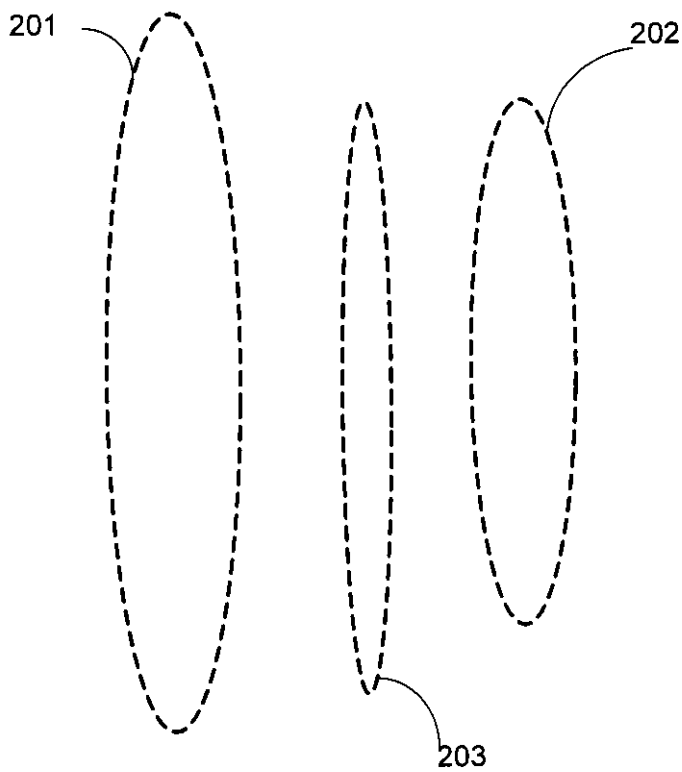


FIG. 2

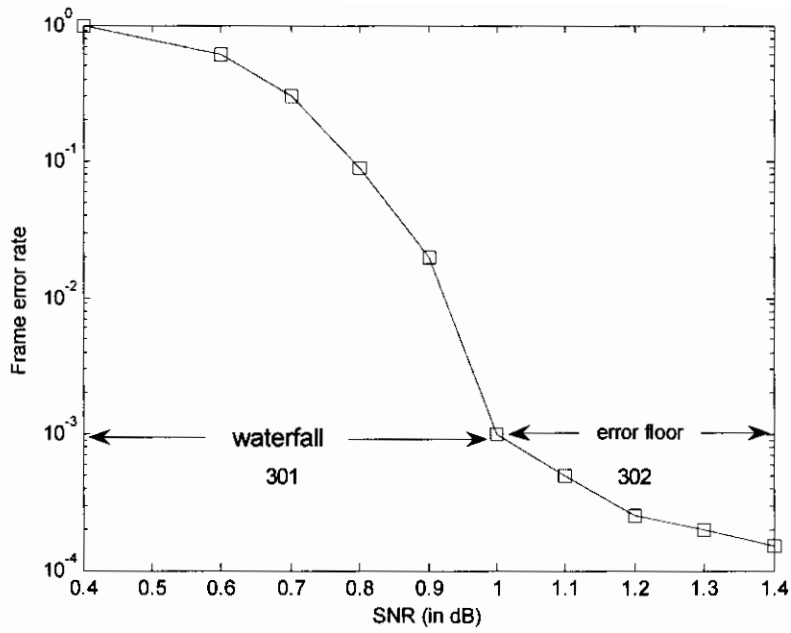

Frame error rate
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
waterfall
301
error floor
302
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
1.2
1.3
1.4
SNR (in dB)

FIG. 3

FIG. 4

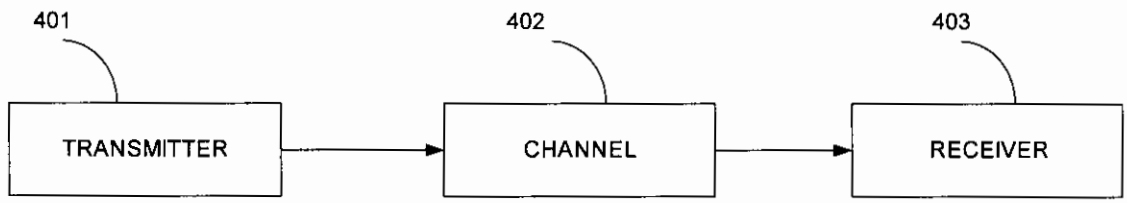
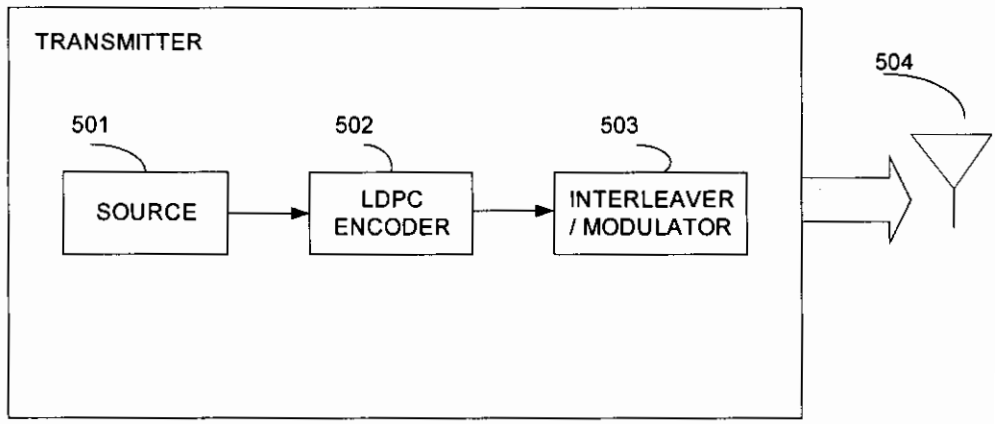


FIG. 5


TRANSMITTER
501
SOURCE
502
LDPC
ENCODER
503
INTERLEAVER
/ MODULATOR
504

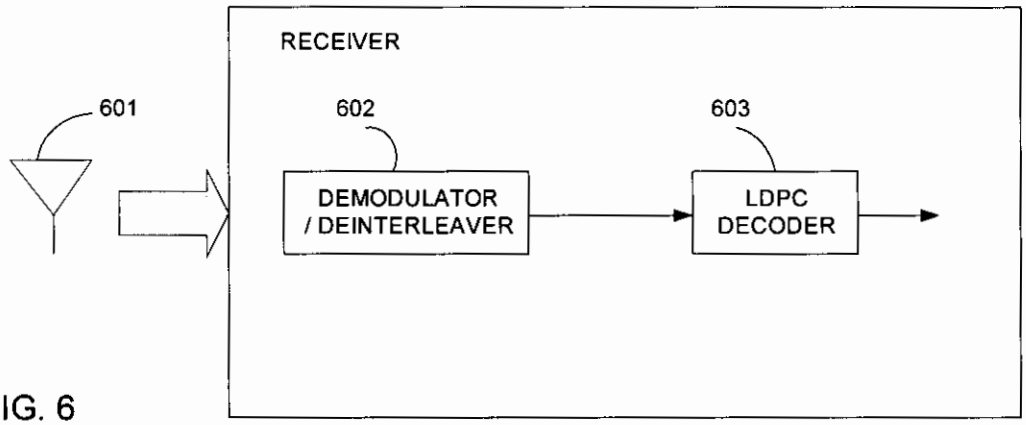

RECEIVER
601
602
DEMODULATOR
/ DEINTERLEAVER
603
LDPC
DECODER

FIG. 6

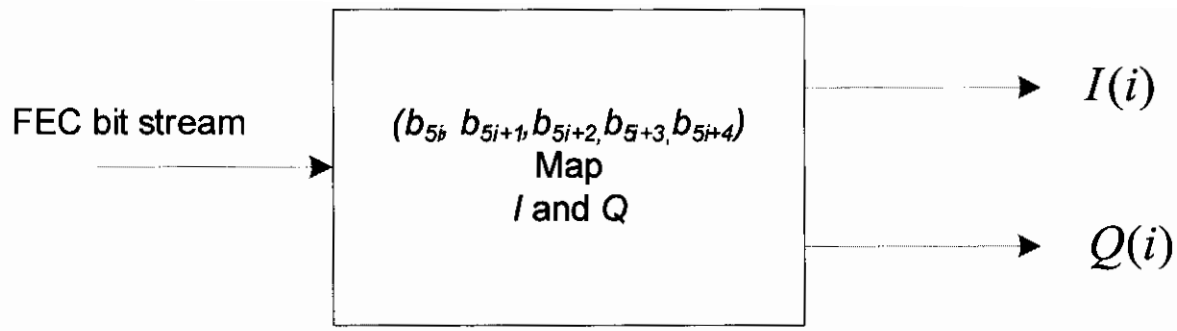


FIG. 7

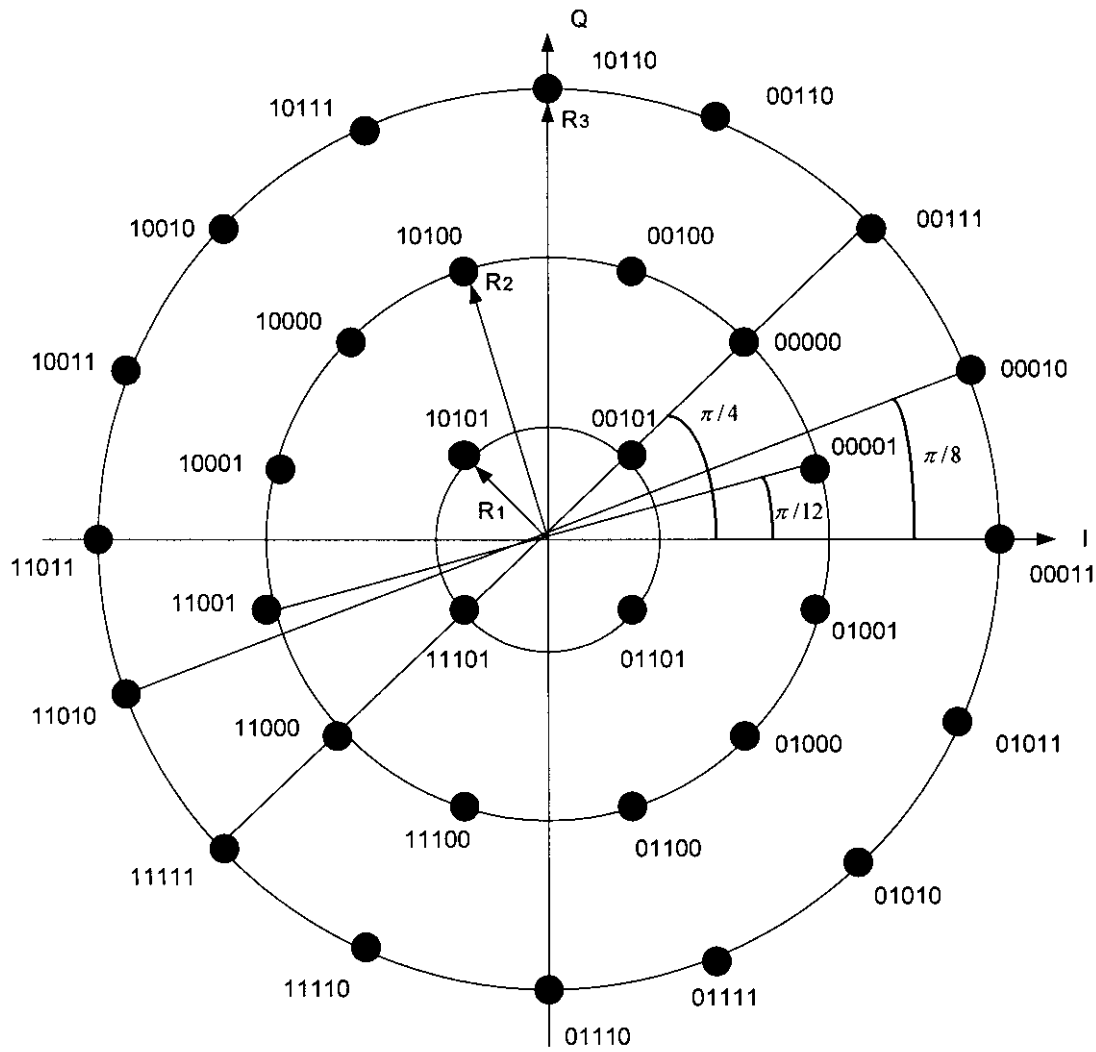

Q
I
10110
00110
10111
00111
10010
10100
00100
R3
R2
10000
00000
10011
00010
10101
00101
π/4
00001
π/8
10001
R1
π/12
11011
00011
11001
01001
11101
01101
11010
11000
01000
01011
11100
01100
11111
01010
11110
01111
01110

FIG. 8