CLAIMS

1. An integrated circuit, comprising:

a photodetection region configured to:

generate, in response to receiving incident photons, charge carriers; and

induce, in a first direction, a first intrinsic electric field;

one or more charge storage regions configured to receive the charge carriers from the photodetection region; and

one or more transfer gates positioned, in the first direction, after the photodetection region and the one or more charge storage regions, and configured to control transfer of charge carriers from the photodetection region to the one or more charge storage regions and/or from the one or more charge storage regions to a readout region.

2. The integrated circuit of claim 1, wherein the photodetection region comprises a first layer having a first intrinsic electric potential level and a second layer positioned, in the first direction, after the first layer and having a second intrinsic electric potential level that is different from the first intrinsic electric potential level.

3. The integrated circuit of claim 2, wherein the first layer has a first dopant concentration the second layer has a second dopant concentration that is higher than the first dopant concentration.

4. The integrated circuit of claim 3, wherein the photodetection region further comprises a third layer positioned, in the first direction, after the second layer and having a third dopant concentration that is higher than the second dopant concentration.

5. The integrated circuit of any one of claims 1-4, wherein the photodetection region comprises a mask having a triangular opening, with a base of the triangular opening positioned, in a second direction, after an apex of the triangular opening, the mask configured to induce, in the second direction, a second intrinsic electric field from the photodetection region to the one or more charge storage regions.

6. The integrated circuit of any one of claims 1-5 or any other preceding claim, wherein the photodetection region has a first intrinsic electric potential level and the one or more charge storage regions have at least a second intrinsic electric potential level that is different from the first intrinsic electric potential level.

7. The integrated circuit of claim 6, wherein the photodetection region has a first dopant concentration and the one or more charge storage regions have at least a second dopant concentration that is higher than the first dopant concentration.

8. The integrated circuit of any one of claims 1-7, further comprising:

one or more charged and/or biased regions configured to induce a charge carrier depletion in the photodetection region for propagating the charge carriers, at least partially in the first direction, from the photodetection region toward the one or more charge storage regions.

9. The integrated circuit of claim 8, wherein the one or more charged and/or biased regions comprise a charge layer comprising a metal-oxide compound that induces the charge carrier depletion in the photodetection region.

10. The integrated circuit of any one of claims 8-9, wherein the one or more charged and/or biased regions comprise:

a first charged and/or biased region positioned on a first side of the photodetection region; and

a second charged and/or biased region positioned on a second side of the photodetection region opposite the first side in a second direction perpendicular to the first direction.

11. The integrated circuit of any one of claims 8-10, wherein the one or more charged and/or biased regions are elongated in the first direction alongside the photodetection region.

12. The integrated circuit of any one of claims 8-11, further comprising one or more transfer gates configured to control transfer of charge carriers between the photodetection region and the one or more charge storage regions and/or between the one or more charge storage regions and a readout region, wherein the one or more transfer gates are positioned, in the first direction, after the photodetection region and the one or more charge storage regions.

13. The integrated circuit of any one of claims 8-12, further comprising one or more doped barriers positioned around the one or more charged and/or biased regions.

14. A method of operating the integrated circuit of any one of claims 1-13, the method comprising:

providing one or more control signals to the one or more transfer gates to control, via the one or more transfer gates, transfer of charge carriers from the photodetection region to the one or more charge storage regions and/or from the one or more charge storage regions to the readout region.

15. A system comprising:

the integrated circuit of any one of claims 1-13; and

a control circuit configured to provide one or more control signals to the one or more transfer gates to control, via the one or more transfer gates, transfer of charge carriers from the photodetection region to the one or more charge storage regions and/or from the one or more charge storage regions to the readout region.