A METHOD OF FABRICATING A COMPOSITE SUBSTRATE

The present invention relates to a method of fabricating a composite substrate of the type comprising an insulating layer that is buried, i.e. interposed between a semiconductor support substrate and an active layer of semiconductor material.

In the description and claims below, the term "insulator" designates an electrically insulating material optionally having a high dielectric permittivity.

More precisely, the invention relates to a method of obtaining a composite substrate as defined above, wherein the insulating layer is thin, i.e. less than 50 nm (50 nanometers) thick, or even less than 20 nm (20 nanometers) thick, with substantially improved electrical properties.

Such a substrate is used in particular in the fields of optics, electronics, and optoelectronics.

A particular but non-limiting example of that type of composite substrate is a substrate known by its acronym "SOI" (silicon on insulator), which designates a substrate comprising a layer of insulating silicon oxide interposed between two layers of silicon.

More precisely, the electrical properties which the method according to embodiments of the invention are intended to improve are:

· the charge density (known by the abbreviation "Qbox") in the buried insulating layer. Obtaining a value of less than 5×10^{11} charges per cm^2 is desirable;

· the breakdown voltage, i.e. the voltage beyond which the resistivity of the insulator falls sharply. Obtaining maximum values is desirable. As an example, for a buried silicon oxide layer, a preferred value is as close to 10 MV/cm [megavolts/centimeter] as possible;

· the mobility of holes and/or electrons in the active layer. As an illustrative example, it would be desirable to obtain an electron mobility of more than 500 $cm^2.V^{-1}.s^{-1}$ [$centimeter^2.volt^{-1}.second^{-1}$] in silicon

doped with boron in a concentration of the order of 10^{15} atoms/cm^3; and

· the "DIT" value, or "density of interface trap", which designates the density of traps at an interface between two layers. In the context of the present invention, an improvement in DIT values at respective interfaces of the buried insulating layer with the neighboring layers is sought.

The remainder of the description focuses on the DIT value as it is one of the principal parameters on which the substrate formation steps of embodiments of the invention have an influence. Further, that parameter has an effect on mobility. However, embodiments of the invention in general aim to improve the electrical performances of the final substrate.

Traps have the capacity to retain or release charge carriers at interfaces. They have an extremely deleterious impact on the electrical properties of electronic components which are to be produced on the composite substrate.

The density of traps at an interface, referred to below as the "DIT value" for simplification, is expressed as the number of traps/$eV.cm^2$. The higher the DIT value, the worse the electrical properties of the substrate.

As an example, a value of 10^{12} $.eV^{-1}.cm^{-2}$ is a high value which corresponds to poor electrical properties for the substrate. Currently, the best DIT values obtained are of the order of 10^{10} $.eV^{-1}.cm^{-2}$ for interfaces between very good quality oxides, known as "gate oxides" and their support. Such oxides are found, for example, in transistors, memories, capacitances and other types of components forming integrated circuits.

Figures 1A to 1E illustrate the various steps of one mode of fabricating an SOI type substrate, which is known in the art.

As shown in Figures 1A and 1B, that method consists of oxidizing a source substrate **Sou** to form a layer of

oxide **Oxy** at its surface, then to carry out atomic species implantation to define an active layer **Cact**. The oxide layer is generally fairly thick, of the order of 150 nm [nanometers].

After bonding to a support substrate **Sup** (Figure 1C) and detaching the remainder of the source substrate **Sou** (Figure 1D), a composite substrate is obtained comprising an oxide layer **Oxy** interposed between a support and an active layer, which has a contact interface with each of the latter, with respective reference numerals I_1 and I_2.

Finally, after fabrication, it may be formed on the upper surface of the composite substrate obtained, a layer intended to protect that surface during finishing heat treatments on the substrate. Hence, the substrate is covered with a protective layer **Cpr** and there is an interface I_3 between that protective layer **Cpr** and the active layer **Cact**.

From the prior art, methods are already known which can improve, i.e. reduce, DIT values, at certain interfaces of a composite substrate. They are principally heat treatments.

One of them, known as "FGA" for "forming gas anneal", consists of carrying out a repair/recovery heat treatment of interfaces at a low temperature, of the order of 450°C, in an atmosphere containing hydrogen and a neutral gas.

However, when such a method is carried out at 450°C, its effect regarding improvement to the DIT value is exerted solely on the interface I_3 between the protective layer Cpr and an active layer **Cact** and not on the interfaces I_1 and I_2, or only very slightly. That FGA treatment method loses effectiveness at each interface which is encountered. Thus, it is relatively ineffective for deep-lying interfaces.

A further possibility consists in carrying out an annealing heat treatment at high temperature, i.e. over 900°C or even over 1000°C. Such a treatment may improve

the DIT value at the interface I_2, but has almost no effect on the interface I_1, which lies deeper.

Further, in many prior applications, a thin buried insulating layer (oxide) is desired, for example less than 50 nm, or even less than 20 nm.

In that case, the oxide no longer plays the role of electrical insulator alone, but forms an integral part of electronic components which are to be formed on the surface of the composite substrate.

Furthermore, the support **Sup**, located at the bottom, no longer has only a mechanical function, but also has an electrical function. Said support substrate **Sup** may optionally contain buried structures, for example a ground plane, or it may be composite.

As a result, improvements to the DIT values at the two interfaces I_1 and I_2, located either side of the buried insulating layer, are desirable.

However, it is well known that producing composite substrates comprising a very thin buried insulating layer is difficult. Hence, for example, for an SOI type substrate, it is known that the thinner the oxide layer, the higher the number of defects inside the final substrate. This is principally due to the presence of contaminants, polluting particles and gas, encapsulated during bonding at the interface I_1.

To improve that bonding, one solution consists of plasma activation of at least one of the surfaces to be bonded, namely that of the support **Sup** and/or insulator **Oxy**. A high bonding energy is thus obtained, close to 1 J/m^2 [joule/meter^2], at the interface I_1, even after an anneal at 200°C for just 2 hours.

However, plasma activation deteriorates the electrical characteristics of the interface I_1, and in particular its DIT values, fairly significantly.

Reference in this regard should be made to the article by K Schjölberg-Henriksen et al, "*Oxide charges induced by plasma activation for wafer bonding*", Sensors

and Actuators A 102 (2002), 99-105, which shows the negative effect of plasma activation on the electrical properties of substrates.

Embodiments of the invention seek to overcome the above-mentioned disadvantages regarding the prior art.

More precisely, embodiments of the invention seek to provide a method of obtaining a composite substrate with a thin buried insulating layer, i.e. thinner than 50 nm, or even thinner than 20 nm, and which may even be as thin as 5 nm, with good electrical properties, i.e. with low DIT values at the two interfaces of said insulating layer.

In accordance with a first aspect of the invention, there is provided a method of fabricating a composite substrate of the type comprising a thin insulating layer, termed the "final layer", interposed between a first semiconductor substrate, termed the "support substrate", and a layer of semiconductor material termed the "active layer", characterized in that it comprises the steps of:

- forming or depositing an insulating layer, termed the "first layer", on said support substrate and an insulating layer, termed the "second layer", on a second substrate, termed the "source substrate";
- plasma activation of at least one of said first and second insulating layers;
- bonding said support substrate and said source substrate together by molecular bonding, such that said first and second insulating layers are in contact along a bonding interface and together form said final insulating layer; and
- lifting off a portion termed the "back" of the source substrate, to retain only a thickness of material constituting said active layer;

the value of the plasma activation energy and the respective thicknesses (e_1, e_2) of the first and second insulating layers being selected such that the activated insulating layer is activated only in its upper portion extending from its free surface, and the thickness of

said final insulating layer is 50 nanometers (50 nm) or less, preferably 20 nanometers (20 nm) or less.

Other advantageous and non-limiting characteristics of the method according to embodiments of the invention, taken alone or in combination, are as follows:

· the thickness (e_1) of the first insulating layer formed or deposited on the support substrate and the thickness (e_2) of the second insulating layer formed or deposited on the source substrate may satisfy the following relationships:

$$e_1 \geq e_{mp1} + d_1 \text{ and } e_2 \geq e_{mp2} + d_2$$

in which e_{mp1} and e_{mp2} respectively correspond to the thickness of the first insulating layer and to the thickness of the second insulating layer the nature of which is modified after the plasma activation treatment, and d_1 and d_2 correspond to the respective tunneling distances of the first and the second insulating layers;

· the first and second insulating layers may have density of interface trap values (DIT) of 10^{11} $eV^{-1}.cm^{-2}$ or less, preferably several 10^{10} $eV^{-1}.cm^{-2}$ or less, at their respective interfaces with the layers on which they are deposited or formed, when these latter are formed from silicon and the insulating layers are formed from silicon dioxide (SiO_2);

· the first insulating layer and/or the second insulating layer may be formed from an oxide or a dielectric material with a high permittivity;

· plasma activation may consist of applying an oxygen plasma to the first and/or the second insulating layer(s) at a flow rate in the range 50 sccm to 200 sccm, a pressure inside the chamber of 50 mTorr, a plasma power of about 250 W for 200 mm substrates and about 500 W for 300 mm substrates, for a period in the range 5 seconds to 60 seconds.

The method may also comprise an annealing step carried out in a mixture of neutral gas and hydrogen, at a temperature close to 900°C, for a period of at least

two hours, on at least one of the two substrates covered with its insulating layer, said step being carried out before plasma activation.

Advantageously, the back portion of the source substrate is lifted off by grinding and/or polishing.

The method may also comprise forming a zone of weakness inside the source substrate, carried out before the plasma activation step, and lifting off the back portion of the source substrate by detachment along said zone of weakness.

Advantageously, said zone of weakness is formed by atomic species implantation in the source substrate. In this latter case, if the above-mentioned annealing step is carried out, it is carried out before the implantation step.

Embodiments of the invention are of particular application to the fabrication of a SOI substrate, in which the source substrate is formed from silicon and the first and second insulating layers are formed from silicon oxide.

In accordance with a second aspect of the invention, there is provided a composite substrate characterized in that it comprises at least one insulating layer interposed between a first semiconductor substrate termed the "support substrate" and a layer of semiconductor material, termed the "active layer", said insulating layer or layers forming an insulating layer termed the "final" layer, having a total thickness of 50 nanometers (50 nm) or less, preferably 20 nanometers or less, and having density of interface trap values (DIT) of $10^{11}.eV^{-1}.cm^{-2}$ or less at its interface with said support substrate and at its interface with said active layer.

Other characteristics and advantages of the invention become apparent from the following description made with reference to the accompanying drawings, which represent a possible implementation and its variations in an indicative but non-limiting manner.

In the drawings:

· Figures 1A to 1E are diagrams representing the various steps in fabrication of an SOI type substrate, in accordance with a known prior art implementation;

· Figures 2A to 2E are diagrams representing the various steps in the fabrication method in accordance with a first implementation of the invention;

· Figures 3A to 3E are diagrams representing a variation of the method illustrated in Figures 2A to 2E;

· Figure 4 is a graph showing the thickness e_{ap} of the insulating layer which is modified after plasma activation treatment as a function of the power density D_P applied to generate said plasma, for two substrates with different diameters; and

· Figure 5 is an enlarged view of Figures 2E and 3E showing the "tunneling" distances.

Figure 2A shows that the method of the invention uses a first substrate 1 termed the "support substrate" and a second substrate 2 termed the "source substrate".

As can be seen in Figure 2B, an insulating layer 31 termed the "first insulating layer" is formed or deposited on the support substrate 1 and an insulating layer 32 termed the "second insulating layer" is formed on the source substrate 2.

The interface between the insulating layer 31 and the support substrate 1 has reference numeral 311 and that between the layers 32 and 2 has reference numeral 321.

The free surfaces of the insulating layers 31, 32 respectively carry reference numerals 310 and 320.

As can best be seen in Figure 2C, plasma activation of at least one of the two insulating layers 31, 32 is then carried out.

Surfaces 310 and 320 are then prepared for bonding carried out by molecular bonding (see Figure 2D).

The bonding interface carries reference numeral 5.

Finally, a portion termed the "back" portion of the source substrate 2 is then lifted off to leave only a

thickness of said material which constitutes an active layer 20, in the final composite substrate with reference numeral 4 (see Figure 2E).

In said composite substrate 4, the substrate 1 acts as a mechanical support, as is usually the case in the prior art.

Further, the support substrate 1 also forms an integral part of electronic components which will subsequently be fabricated on the surface of the composite substrate 4. In the context of the invention, wherein a material with a low DIT value is to be obtained at the interface 311 between the insulator 31 and the support substrate 1, the nature and the physical characteristics of the material constituting said support substrate 1 have an influence on the electrical performances of said electronic components. For this reason, the support substrate 1 is advantageously formed from a semiconductor material.

Further, it is even possible for said support substrate 1 to contain elements which will be constituents of the final electronic components (such as electrodes, a ground plane, a channel, etc)

Finally, it is also possible to have, as the support substrate 1, a composite substrate in order to produce a multi-layer structure. Purely by way of illustrative example, a bulk silicon substrate with an epitaxial layer of silicon germanium (SiGe) containing 20% of germanium may act as a support substrate.

The active layer 20 of the composite substrate 4 is derived from source substrate 2 as is described below. Said source substrate 2 is also formed from semiconductor material.

Purely by way of illustrative example, various examples of materials which may be used as substrates 1 and 2 are mentioned below:

- support substrate 1: silicon (Si), silicon carbide (SiC), germanium (Ge), any epitaxially grown layer, for

example a layer of germanium (Ge), silicon germanium (SiGe) or gallium nitride (GaN) on a silicon substrate, or even a layer of strained silicon;

· source substrate 2: silicon (Si), germanium (Ge), silicon carbide (SiC), gallium nitride (GaN), silicon germanium (SiGe), gallium arsenide (AsGa) or indium phosphide (InP).

The insulating layers 31, 32 are selected, for example, from layers of oxide or nitride, such as silicon oxide (SiO_2) or silicon nitride (Si_3N_4); germanium oxynitride ($Ge_xO_yN_z$); high permittivity (high k) dielectric materials such as hafnium dioxide (HfO_2), yttrium oxide (Y_2O_3), strontium and titanium trioxide ($SrTiO_3$), alumina (Al_2O_3), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), their nitrides and their silicides.

The nature of each insulating layer 31 or 32 is selected firstly to optimize the electrical performances of interfaces 311 and 321, and secondly as a function of the nature of the materials used for the support substrate 1 and the source substrate 2. By way of example, to produce a final substrate 4 of the GeOI (germanium on insulator) type, a thin layer of silicon oxide may be formed on the silicon support substrate and a layer of HfO_2 on the germanium source substrate.

Preferably, the insulators 31, 32 are of excellent quality as regards their electrical properties. More precisely, they have DIT values at interfaces 311 and 321 which are as low as possible.

By way of illustrative example, when the layers 1 and 2 are formed from silicon and the insulating layers 31, 32 are formed from silicon dioxide, the DIT values at interfaces 311 and 321 are $10^{11}.eV^{-1}.cm^{-2}$ or less, or even $10^{10}.eV^{-1}.cm^{-2}$ or less.

Next, when the insulator is an oxide, it is formed with all precautions taken to form oxides of optimum quality, such as gate oxides. Reference in this regard

could be made to the article by Green et al, "*Ultrathin (<4nm) SiO_2 and Si-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure and physical and electrical limits*", Journal of Applied Physics, volume 90, n° 5, September 1, 2001, pages 2086 ff.

The surfaces of substrates 1 and 2 on which the oxide is to be formed are prepared by deep cleaning, for example using a treatment in an "RCA" chemical, to prevent any contamination.

"RCA" treatment consists of treating the surfaces in succession with the following:

· a first solution known by the acronym "SC1" (standard clean 1), which comprises a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water;

· a second solution known by the acronym "SC2" (standard clean 2), which comprises a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionized water.

The oxides are then obtained by an oxidation heat treatment respectively of the support substrate 1 and/or the source substrate 2, optionally followed by a post-oxidation treatment of the "forming gas anneal" (FGA) type.

The insulating layers 31, 32 may also be obtained by low pressure chemical vapor deposition (LPCVD) or by an atomic layer deposition (ALD) method.

Said deposition may optionally be preceded by a surface passivation treatment of substrates 1 or 2. As an example, said treatment may consist of forming several silicon dioxide (SiO_2) monolayers on silicon prior to depositing an insulating layer 31 or 32 of hafnium dioxide (HfO_2).

The characteristics of the thicknesses e_1 and e_2 of the insulating layers 31, 32 are described below.

The plasma activation treatment (Figure 2C) is carried out under conditions which preserve the electrical characteristics and in particular the DIT values of the interface between the insulating layer and the neighboring layer.

"Plasma activation" of a surface is defined as exposing that surface to a plasma, which may in particular be carried out in a chamber under vacuum or at atmospheric pressure.

Said activation is carried out by controlling various exposure parameters such as the nature, the flow rate or the pressure of the gas supplied to the chamber inside which activation is carried out, as well as the applied power.

In the context of the invention, the substrate covered with the insulating layer to be activated is introduced into the chamber, then a pure gas, typically oxygen (O_2), optionally nitrogen (N_2), argon (Ar) or helium (He) or a mixture of said gases, such as oxygen and helium, oxygen and argon or helium and nitrogen, for example, is sent into the chamber.

The flow rate of the gas used is a function of the volume of the activation chamber and the size of the substrate.

Preferably, the gas is sent in at a flow rate in the range 10 sccm to 1000 sccm (standard cubic centimeter per minute), typically in the range 50 sccm to 200 sccm. By way of example, a flow rate of 75 sccm for a 200 mm diameter substrate is used, while a flow rate of 200 sccm is used for a 300 mm diameter substrate.

The pressure established in the chamber during plasma treatment is controlled, so that it is in the range 10 mTorr to 200 mTorr, typically close to 50 mTorr (1 mTorr being equal to 1.33×10^{-1} Pa).

The plasma is initiated then maintained by application of a RF power (radiofrequency) in the range 100 W to 2000 W, preferably close to 250 W in the case of

200 mm diameter substrates and in the range 100 W to 3000 W, preferably close to 500 W in the case of 300 mm diameter substrates.

The surface of the insulator is then exposed to plasma for 5 to 60 seconds, preferably 10 to 30 seconds.

During plasma treatment, the surfaces 310 and/or 320 of the insulators undergo ionic bombardment which modifies the treated insulator over a thickness e_{mp} (thickness modified by plasma treatment).

These thicknesses, with references e_{mp1} or e_{mp2} depending on whether they concern the first insulating layer 31 or the second 32, may be adjusted as a function of the power used to apply the plasma and the exposure time for that plasma.

Each insulating layer 31, 32 is then modified solely in its upper portion, i.e. the portion in the figures which extends from the free surface 310 or, respectively, 320.

Measurements were carried out to determine the thickness e_{mp} of the insulating layer which is modified by the plasma treatment, as a function of the density D_P of the power of the applied plasma, expressed in W/cm^2, for a period of 30 seconds. These measurements were carried out on a layer of silicon oxide, the plasma being an oxygen plasma. The results obtained are shown in the accompanying Figure 4.

The results represented as a triangle correspond to those obtained with substrates with a diameter of 200 mm, and those represented by a diamond correspond to those for 300 mm diameter substrates.

These results show that the plasma treatment may result in a modification to the nature of the oxide layer over a thickness of 8 nm. Complementary measurements have shown that this thickness may be greater, for example for a higher power density.

As a result, to prevent the plasma treatment from affecting the DIT values of the interfaces 311, 321, it

is necessary to form an insulating layer the thickness e_1 or e_2 of which is greater than the respective thicknesses e_{mp1} and e_{mp2} modified by the plasma.

Hence, preferably, the thicknesses e_1 and e_2 of the insulating layers 31, 32 satisfy the following relationships:

$$e_1 \geq e_{mp1} + d_1$$

$$e_2 \geq e_{mp2} + d_2$$

in which d_1 and d_2 respectively represent the "tunneling" distances of the first and second insulating layer 31, 32.

Each insulator is thus thicker than the portion which can be perturbed by the plasma treatment, taking at least the tunneling distance as a safety thickness.

In the remainder of the description and claims, the tunneling distance d_1 (respectively d_2) is defined as being the distance from the interface 311, respectively 321, beyond which the traps or defects created by the plasma are not capable of being charged by the "tunneling" effect when the electronic component fabricated from composite substrate 4 is used.

An enlarged view of the tunneling distances d_1 and d_2 is shown in Figure 5.

In other words, the defects created are sufficiently far away from the interface 311 or 321 to have no significant influence thereon. The tunneling distance d_1 or d_2 depends on the nature of the materials constituting the insulator, the source and support substrates, and also depend on the types of electronic components produced (since the tunneling distance depends on the electric field around the interface).

The skilled person will be able to determine the value of d_1 and d_2 depending on the values of these parameters. As an example, the tunneling distance is approximately 2 nm for an oxide of Si (SiO_2) on silicon, in the voltage range used in CMOS technology.

Further, the thickness e_1 of the first insulating layer 31 and the thickness e_2 of the second insulating layer 32 are determined so that the total thickness of the final insulating layer 3 of the composite substrate 4 preferably does not exceed 50 nm or more preferably 20 nm. The thickness of this final layer 3 approximately corresponds to the sum of e_1 and e_2. However, it should be noted that it is also possible to thin one or both of the insulating layers 31, 32 slightly, after the plasma treatment and before bonding. This thinning step is described below.

Finally, when the insulating layer used is a high dielectric permittivity material, i.e. a material for which the relative permittivity ϵ_r is significantly higher than that of SiO_2 (for which ϵ_r is close to 3.9), it is routine to convert its thickness e into the "equivalent oxide thickness", "EOT", using the formula:

$$EOT = (\epsilon_{SiO2}/\ \epsilon_r).e$$

Insofar as the invention is applicable to forming a thin insulating layer 3 (<50 nm) regardless of its nature, it is understood that if this insulating layer is formed by a layer with a high dielectric permittivity, this can result in a very low EOT.

It is also appropriate to limit the exposure time for the plasma treatment to what is strictly necessary.

Preferably, this is less than one minute, or better still less than 30 seconds. Prolonged exposure would risk causing an accumulation of electric charges in the insulator and an increase in the charge density of the insulator (QBOX), which will counter the improvements in electrical performances discussed in the introduction.

Respective management of plasma activation treatment parameters and the thicknesses of the two insulating layers 31 and 32 can guarantee that the defects created by the plasma treatment will be far away from interfaces 311 or, respectively, 321.

In the implementation illustrated in Figures 2D and 2E, the back portion of the source substrate 2 is lifted off by grinding and/or polishing.

A variation of this method is described with reference to Figures 3A to 3E. Only those steps which have been modified, concerning lifting off the back portion, are described in detail.

As can be seen in Figure 3B, a zone of weakness 22 is formed within a source substrate 2. Said zone of weakness delimits the active layer 20 from the back portion 21 of substrate 2.

The zone 22 may be formed by a porous zone; in this regard, reference should be made to the article by K Sakaguchi et al, *"Eltran® by splitting porous Si layers"*, The ElectroChemical Society Inc PV99-3, Silicon-on-insulator technology and devices, P.L. Hemment, pp 117-121. In this case, the porous zone is formed prior to depositing the layer 32.

The zone 22 is advantageously formed by implantation of light atomic species, preferably hydrogen and/or helium ions, so as not to deteriorate the thin oxide 32.

Reference should be made to the article by C. Maleville and C. Mazuré, *"Smart Cut™ technology: from 300 nm ultrathin SOI production to advanced engineered substrates"*, Solid State Electronics 48 (2004), 1055-1063, for implantation conditions.

It should be noted that, although it is not shown in the figures, it is also possible to carry out the atomic species implantation step taking care to deposit or form a protective layer of oxide or nitride on the insulating layer 32.

The nature of said additional protective layer is selected so as to facilitate its selective lifting off, without ruining the subjacent insulating layer. This lifting off may, for example, be carried out by selective etching.

As an example, if the insulator formed is SiO_2, it is possible to deposit a protective layer of silicon nitride (Si_3N_4). This protective layer will subsequently be eliminated prior to the bonding step.

If said protective layer is retained during plasma activation, its thickness should be taken into account when selecting the suitable plasma power.

Said power may be selected to be higher, all the while paying attention to the tunneling distance, said higher power in some cases producing higher energy bonding.

The plasma activation and bonding steps are then carried out as described above (see Figures 3C, 3D).

Prior to carrying out the plasma treatment, specific cleaning precautions are taken to ensure the elimination of particles and metallic contaminants which can generate defects, for example charges in the insulator (QBOX). To clean SiO_2 surfaces, as described above, a "RCA" solution is used, this solution comprising a step for cleaning using a SC2 solution (which is known to eliminate these contaminants).

Finally, as shown in Figure 3E, the step for detaching the back portion 21 along the zone 22 consists of applying stresses of thermal or mechanical origin, for example an anneal or introduction of a blade at said zone of weakness 22.

In a variation of the two above-mentioned implementations, described with reference to Figures 2 and 3, in particular if a very thin insulating layer (of the order of 5 nm) is to be made, the insulating layer or layers 31, 32 may be thinned after the plasma treatment and prior to bonding.

Care is taken not to lift off a thickness beyond which the "strong bonding" effect of the plasma would be lost. Hence, it is known that beyond a thinning of 5 to 10 Angstroms in a layer of SiO_2 activated by plasma, this effect starts to disappear. It disappears completely

upon thinning beyond 40 Angstroms. In the case of SiO_2, a SC1 solution may be used to etch and eliminate a selected thickness of oxide. This step based on SC1 can combine the effects of cleaning and etching of this solution.

In another variation of the two above-mentioned methods, described with reference to Figures 2 and 3, after forming insulating layers 31, 32 and prior to the plasma activation step and prior to any atomic species implantation, it is also possible to carry out forming gas anneal type treatment, "FGA".

Said "FGA" heat treatment is advantageously carried out in a neutral gas and hydrogen atmosphere at a temperature close to 450°C for a period in the range from about 30 minutes to several hours.

It is also possible to carry out a heat treatment in a neutral gas at a higher temperature, for example over 900°C for SiO_2, in argon.

Said heat treatments may be carried out on one or the other or both substrates 1 and 2.

The method of the invention has the advantage of producing the bonding interface 5 at a sufficiently large distance from the two interfaces 311 and 321, thus retaining low density of interface trap values (DIT).

In accordance with the invention, it is also important to form an insulating layer 31, 32 on each of substrates 1, 2 to be bonded, as otherwise the bonding interface which would then exist between the insulator and the substrate not covered with insulator would have DIT values which were too high and would thus have mediocre electrical properties, which are insufficient for the envisaged applications.

Some particular examples of implementations is described below.

EXAMPLE 1: Preparation of an SOI type substrate with an oxide layer thickness of 25 nm

Thermal oxidation of a 200 mm diameter silicon substrate was carried out to form thereon a 10 nm thick insulating layer of silicon oxide (SiO_2).

In a similar manner, a 15 nm thick silicon oxide layer was formed on a silicon source substrate of the same size.

Next, the two substrates underwent "FGA" type annealing heat treatment to arrive at the electrical properties of the two oxides.

The silicon source substrate then underwent a hydrogen ion implantation step, carried out through the silicon oxide layer covering it. Implantation was carried out at a dose of 5.5×10^{16} H^+/cm^2 using an implantation energy of 35 keV.

Next, the upper surface of said substrate was cleaned with a SC1 solution then with SC2 in succession.

The silicon oxide layer of the source substrate thus prepared then underwent an oxygen plasma activation treatment applied for 30 seconds at a power density of 0.8 W/cm^2, at an oxygen pressure of 50 mTorr (6.66 Pa), a flow of 75 sccm (standard cubic centimeter), at 20°C.

Plasma activation modified the nature of the oxide layer over a maximum thickness of 5.5 nm. It was thus observed that the thickness of the oxide, which was 15 nm, was substantially greater than the thickness treated by the plasma plus the tunneling distance **d**, which was 2 nm. Thus, the above-mentioned mathematical relationship is satisfied.

The surfaces to be brought into contact were then cleaned by rinsing with chemicals and/or scrubbing, then bonded by molecular bonding.

Finally, heat treatment was carried out for several hours at a temperature in the range 350°C to 600°C to separate and detach the back portion of the source substrate from the active layer.

After detachment, the surface of the SOI substrate was finished (i.e. steps of stabilization, thinning and polishing).

The DIT values of interfaces 311 and 321 prior to the plasma activation treatment were respectively of the order of a few $10^{10}.eV^{-1}.cm^{-2}$.

The final composite substrate obtained had DIT values of the same order of magnitude for interfaces 311 and 321 respectively.

Identical results were obtained for 300 mm diameter silicon substrates using a flow of 150 sccm (standard cubic centimeter).

EXAMPLE 2: Preparation of an SOI type substrate with an oxide thickness of 11 nm

The procedure of Example 1 was used, respectively with oxide thicknesses of 3 nm on the support substrate and 10 nm on the source substrate. The oxides obtained were then treated at 450°C for about 1 hour in an atmosphere formed by 2% hydrogen in argon (FGA treatment, forming gas anneal) to improve the DIT values.

The source substrate, which comprised the thickest oxide layer, was activated by plasma at a power of 2 W/cm^2, resulting in a modification of the oxide over about 7 nm.

This plasma treated insulating layer was cleaned in a SC1 solution using a concentration, temperature and time sufficient to etch it over a depth of the order of 2 nm.

The final composite substrate obtained was an SOI type structure which comprised a buried insulating layer with a thickness of the order of 11 nm and which had good electrical qualities, in particular a DIT of the order of several $10^{10}.eV^{-1}.cm^{-2}$.

EXAMPLE 3: Preparation of a GeOI type substrate with an oxide thickness of 20 nm

A 5 nm layer of HfO_2 was formed on a 200 mm diameter source substrate of bulk germanium. In a variation, the source substrate may consist of a 200 mm silicon wafer on which a layer of germanium has been formed by epitaxy.

A 15 nm layer of silicon oxide (SiO_2) was formed on a silicon (Si) support substrate.

The silicon oxide layer of the support substrate then underwent an oxygen plasma activation treatment applied for 30 seconds with a power density of 0.4 W/cm^2 at an oxygen pressure of 50 mTorr (6.66 Pa), with a flow rate of 75 sccm, at 20°C.

Bonding was then carried out followed by lifting off the upper portion of the germanium source substrate by detachment using the SmartCut™ method. A GeOI substrate was obtained with a DIT value of the order of several $10^{11}.eV^{-1}.cm^{-2}$ at the interface with the germanium and several $10^{10}.eV^{-1}.cm^{-2}$ at the interface with the silicon.

It should be noted that the DIT value obtained is higher than in the preceding examples, because currently, the surface preparation of germanium (Ge) and the selection of suitable insulators for these materials have not been completely mastered. It is possible that in the future, a more judicious choice of surface treatments and materials selected as insulators and their formation conditions might result in lower DIT values. The invention proposed here can be adapted to the change in the technology.

EXAMPLE 4: Preparation of a composite substrate

The procedure of Example 3 was carried out, except that the support substrate was not a bulk silicon substrate but a hybrid SOI type substrate. It was formed from a silicon support substrate, a 150 nm buried SiO_2 layer and a superficial 100 nm layer of silicon (Si).

The superficial layer of said hybrid support substrate was oxidized over about 10 nm to form a silicon oxide with a thickness of the order of 20 nm.

Next, plasma activation, bonding and lifting off the back portion of the source substrate were carried out as described in the preceding example. Finally, a composite structure was formed with the following structure, in succession:

- the support substrate;
- a 150 nm silicon oxide insulator;
- a 90 nm Si layer;
- a 20 nm oxide layer;
- a 5 nm HfO_2 layer;
- a final Ge layer.

EXAMPLE 5: Preparation of a double SOI type substrate wherein each of the buried insulating layers is thin

Example 1 was carried out once, then a second time using as the support substrate the SOI substrate obtained the first time at the end of the method of Example 1.

A composite substrate was thus obtained containing, in succession:

- the support substrate;
- a 25 nm silicon oxide insulator;
- a 50 nm Si layer;
- a 25 nm silicon oxide layer;
- a 50 nm final silicon layer.

The composite substrates obtained in accordance with Examples 4 and 5 had good electrical performances at each of its interfaces, even the deepest, which could not be achieved with a final FGA type treatment.

CLAIMS

1. A method of fabricating a composite substrate of the type comprising at least one thin insulating layer, termed the "final layer", interposed between a first semiconductor substrate, termed the "support substrate", and a layer of semiconductor material, termed the "active layer", characterized in that it comprises the steps of:

- forming or depositing an insulating layer, termed the "first layer", on said support substrate and an insulating layer, termed the "second layer", on a second substrate, termed the "source substrate";

- plasma activation of at least one of said first and second insulating layers;

- bonding said support substrate and said source substrate together by molecular bonding, such that said first and second insulating layers are in contact along a bonding interface and together form said final insulating layer; and

- lifting off a portion, termed the "back", of the source substrate, to retain only the thickness of material constituting said active layer;

the value of the plasma activation energy and the respective thicknesses (e_1, e_2) of the first and second insulating layers being selected such that the activated insulating layer is activated only in its upper portion extending from its free surface, and the thickness of said final insulating layer is 50 nanometers (50 nm) or less.

2. A method according to claim 1, characterized in that the thickness (e_1) of the first insulating layer formed or deposited on the support substrate and the thickness (e_2) of the second insulating layer formed or deposited on the source substrate satisfy the following relationships:

$$e_1 \geq e_{mp1} + d_1 \text{ and } e_2 \geq e_{mp2} + d_2$$

in which e_{mp1} and e_{mp2} respectively correspond to the thickness of the first insulating layer and to the thickness of the second insulating layer the nature of which is modified after the plasma activation treatment, and d_1 and d_2 correspond to the respective "tunneling" distances of the first and the second insulating layers.

3. A method according to claim 1 or claim 2, characterized in that the first and second insulating layers have density of interface trap (DIT) values of 10^{11} $eV^{-1}.cm^{-2}$ or less, preferably several 10^{10} $eV^{-1}.cm^{-2}$ or less, at their respective interfaces with the layers on which they are deposited or formed, when these latter are formed from silicon and the insulating layers are formed from silicon dioxide (SiO_2).

4. A method according to any preceding claim, characterized in that the first insulating layer and/or the second insulating layer is/are an oxide.

5. A method according to any preceding claim, characterized in that the first insulating layer and/or the second insulating layer is/are a high permittivity dielectric material.

6. A method according to claim 5, characterized in that the high permittivity dielectric material is selected from the group comprising hafnium dioxide (HfO_2), yttrium oxide (Y_2O_3), strontium and titanium trioxide ($SrTiO_3$), alumina (Al_2O_3), zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), titanium dioxide (TiO_2), their nitrides and their silicides.

7. A method according to claim 4, characterized in that the first and/or the second oxide layer(s) are

obtained by thermal oxidation of the support substrate and/or the source substrate respectively.

8. A method according to any preceding claim, characterized in that plasma activation consists of applying an oxygen plasma to the first and/or the second insulating layer(s) at a flow rate in the range 50 sccm to 200 sccm, a pressure inside the chamber of 50 mTorr, a plasma power of about 250 W for 200 mm substrates and about 500 W for 300 mm substrates, for a period in the range 5 seconds to 60 seconds.

9. A method according to any preceding claim, characterized in that it further comprises an annealing step carried out in a mixture of neutral gas and hydrogen, at a temperature close to 900°C, for a period of at least two hours, on at least one of the two substrates covered with its insulating layer, said step being carried out before plasma activation.

10. A method according to any preceding claim, characterized in that the back portion of the source substrate is lifted off by grinding and/or polishing.

11. A method according to any one of claims 1 to 9, characterized in that it comprises forming a zone of weakness inside the source substrate, carried out before the plasma activation step and lifting off the back portion of the source substrate by detachment along said zone of weakness.

12. A method according to claim 11, characterized in that it consists, after forming the second insulating layer, in carrying out a step for atomic species implantation into the source substrate to define therein said zone of weakness.

13. A method according to claims 9 and 12, characterized in that the annealing step in neutral gas and in hydrogen is carried out prior to the atomic species implantation step.

14. A method according to any preceding claim, characterized in that it comprises a step for thinning at least one of the first and second insulating layers, carried out after plasma activation and prior to bonding.

15. A method of fabricating an SOI type substrate according to any preceding claim, characterized in that the source substrate is formed from silicon and the first and second insulating layers are formed from silicon oxide.

16. A method according to any preceding claim, characterized in that the thickness of said final insulating layer is 20 nanometers (20 nm) or less.

17. A composite substrate, characterized in that it comprises at least one insulating layer interposed between a first semiconductor substrate, termed the "support substrate", and a layer of semiconductor material, termed the "active layer", said insulating layer or layers forming an insulating layer, termed the "final" layer, having a total thickness of 50 nanometers (50 nm) or less, and having density of interface trap (DIT) values of $10^{11}.eV^{-1}.cm^{-2}$ or less at its interface with said support substrate and at its interface with said active layer.

18. A composite substrate according to claim 17, characterized in that said insulating layer or layers are formed from an oxide.

19. A composite substrate according to claim 17 or claim 18, characterized in that said insulating layer or layers are formed from a high permittivity dielectric material.

20. A composite substrate according to any one of claims 17 to 19, characterized in that the active layer is produced from a material selected from silicon (Si), germanium (Ge), silicon carbide (SiC), gallium nitride (GaN) and silicon germanium (SiGe).

21. A composite substrate according to any one of claims 17 to 20, characterized in that the total thickness of said final insulating layer is 20 nanometers (20 nm) or less.

22. A composite substrate according to any one of claims 17 to 21, characterized in that said final insulating layer has density of interface trap (DIT) values of several $10^{10}.eV^{-1}.cm^{-2}$ or less.

A METHOD OF FABRICATING A COMPOSITE SUBSTRATE

Abstract

The invention concerns a method of fabricating a composite substrate (4) of the type comprising at least one thin final insulating layer (3) interposed between a support substrate (1) and an active layer (20) of semiconductor materials.

It is remarkable in that it comprises:

- forming or depositing an insulating layer (31) on said support substrate (1) and an insulating layer (32) on a source substrate (2);
- plasma activation of at least one of said insulating layers;
- bonding the two substrates (1, 2) by molecular bonding via their respective insulating layers; and
- lifting off a back portion (21) from the source substrate (2), to retain only said active layer (20);

the value of the plasma activation energy and the respective thicknesses (e_1, e_2) of the insulating layers (31, 32) being selected such that the activated insulating layer is activated only in its upper portion, and the thickness of said final insulating layer (3) is 50 nanometers (50 nm) or less.

FIGURE 2E