FIG. 1A

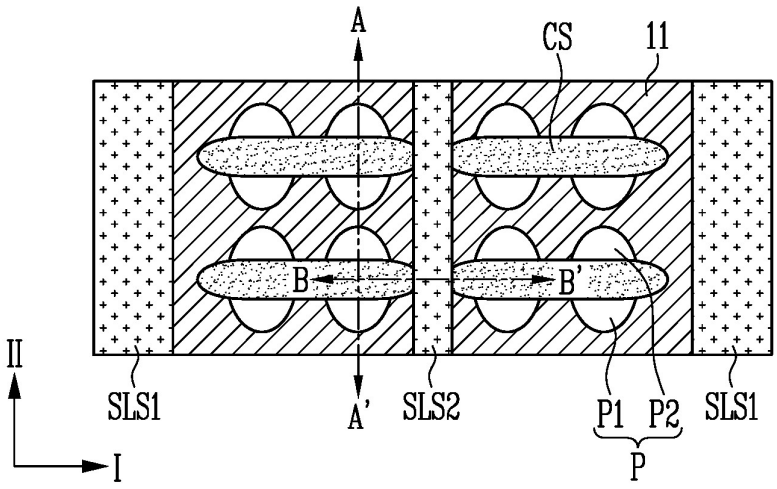


FIG. 1B

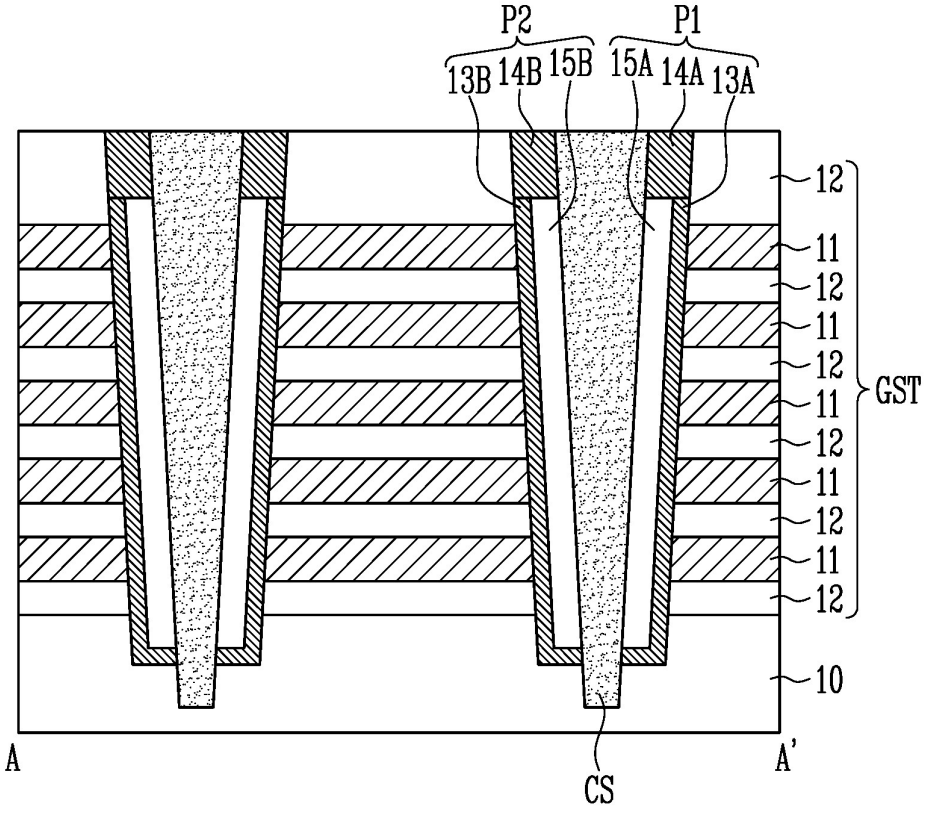

P2
P1
13B
14B
15B
15A
14A
13A
12
11
12
11
12
11
12
11
12
11
12
GST
10
A
A'
CS

FIG. 1C

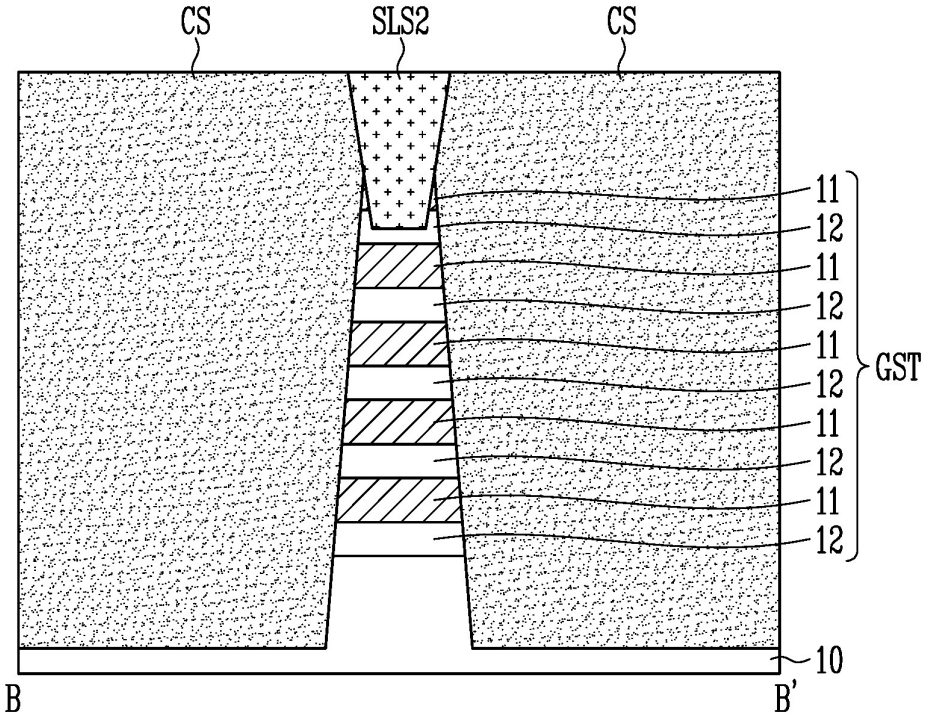


FIG. 1D

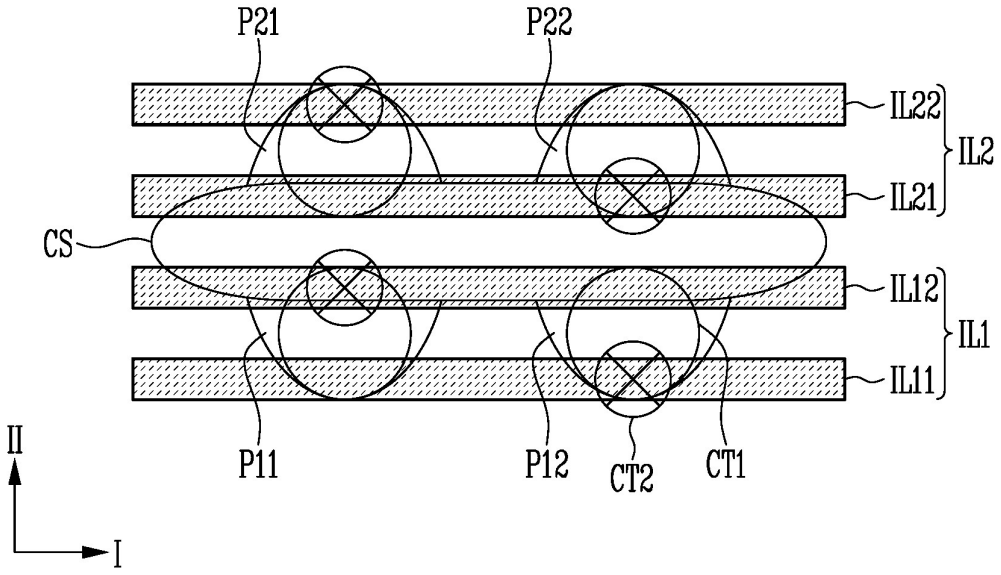

P21
P22
IL22
IL2
IL21
CS
IL12
IL1
IL11
II
P11
P12
CT2
CT1
I

FIG. 2A

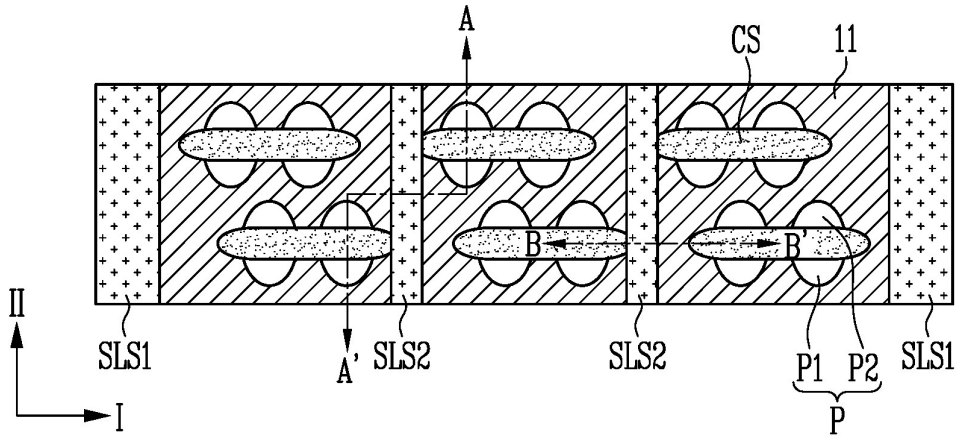

A
CS
11
B
B'
II
SLS1
A'
SLS2
SLS2
P1
P2
SLS1
P
I

FIG. 2B

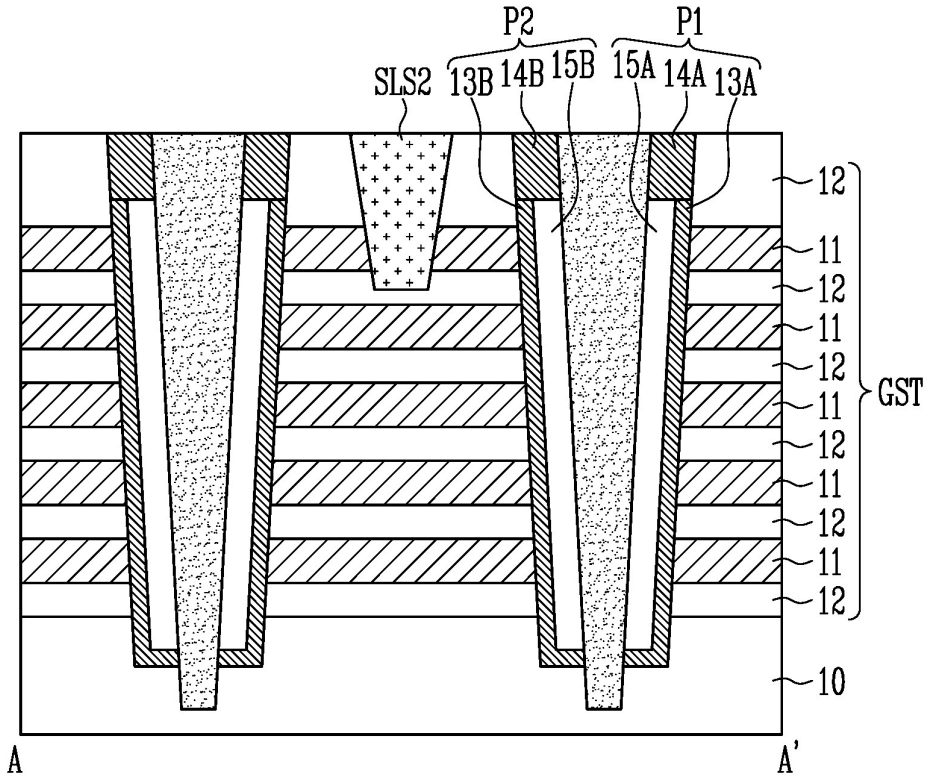

P2
P1
SLS2
13B
14B
15B
15A
14A
13A
12
11
12
11
12
11
12
11
12
11
12
GST
10
A
A'

FIG. 2C

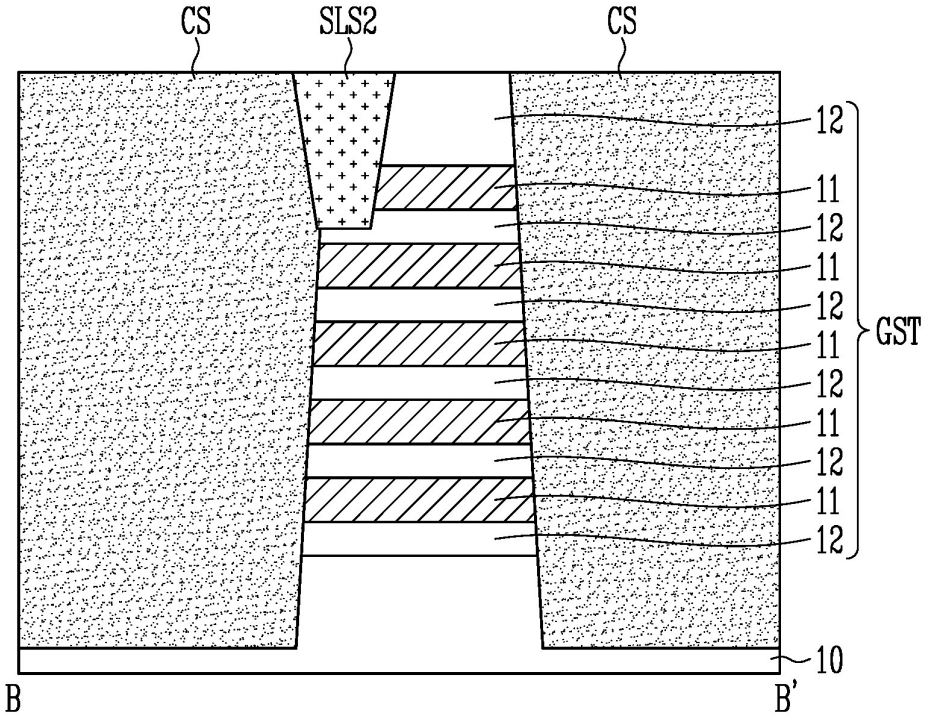

CS
SLS2
CS
12
11
12
11
12
11
12
11
12
11
12
GST
10
B
B'

FIG. 3A

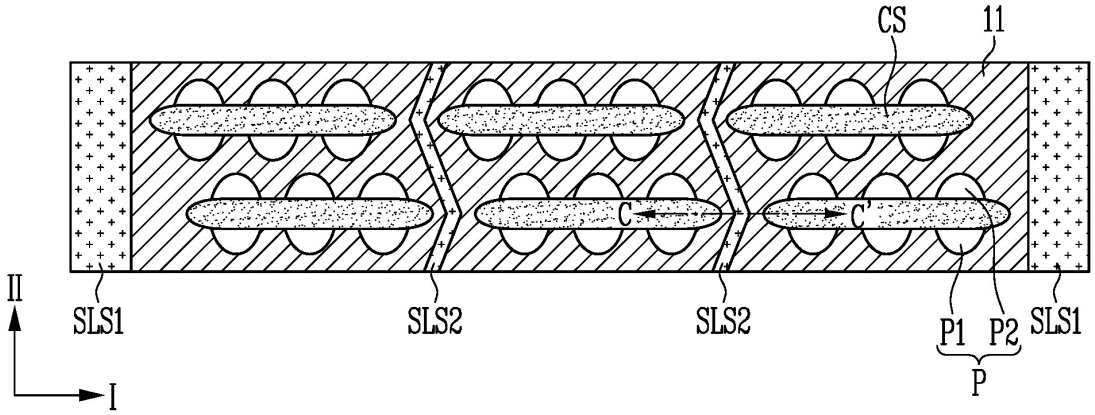

CS
11
C
C'
II
I
SLS1
SLS2
SLS2
P1
P2
P
SLS1

FIG. 3B

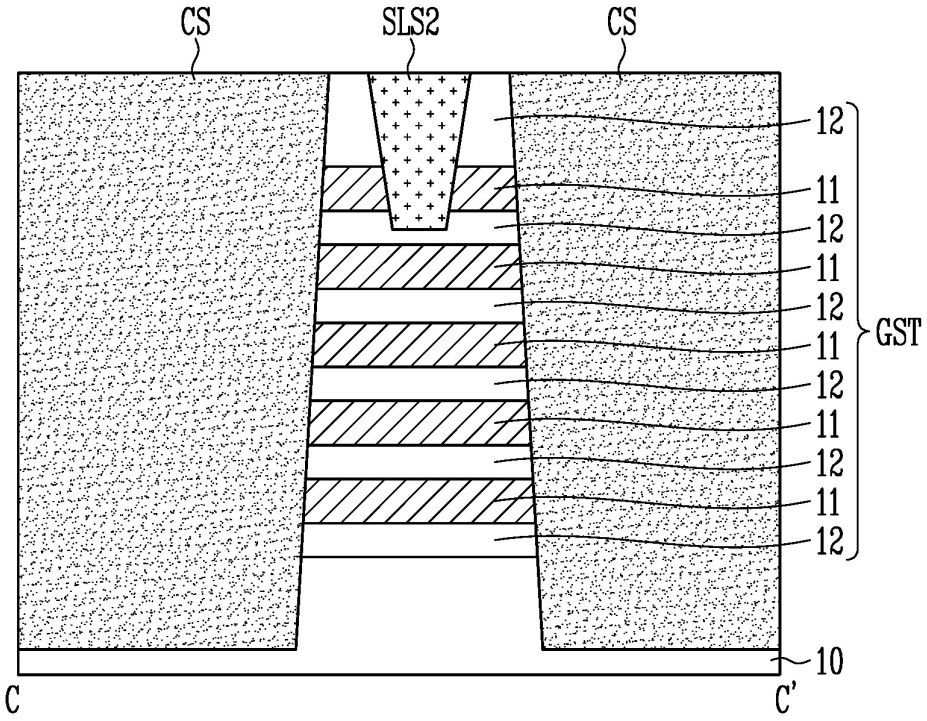

CS
SLS2
CS
12
11
12
11
12
11
12
11
12
11
12
GST
10
C
C'

FIG. 3C

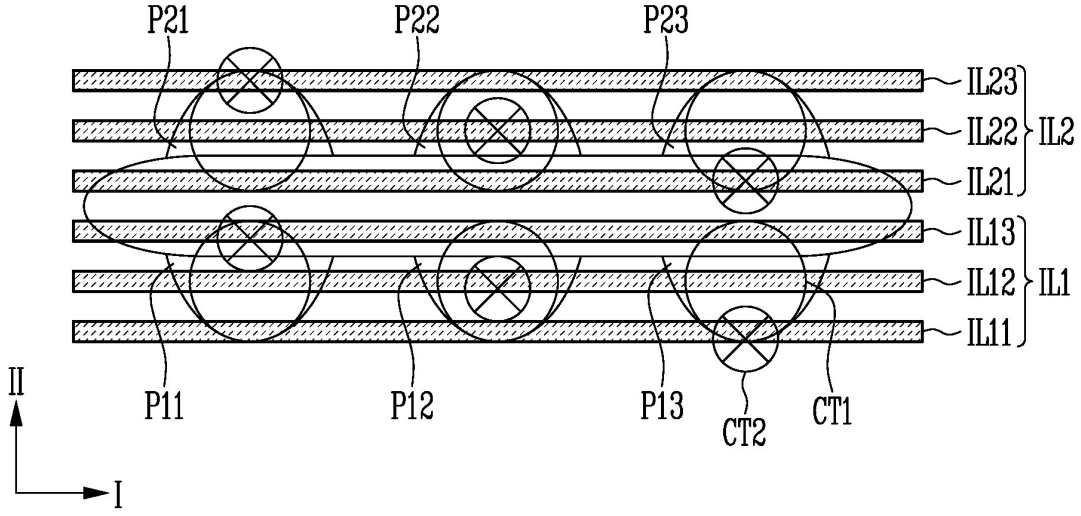

P21
P22
P23
IL23
IL22
IL2
IL21
IL13
IL12
IL1
IL11
II
P11
P12
P13
CT2
CT1
I

FIG. 4A

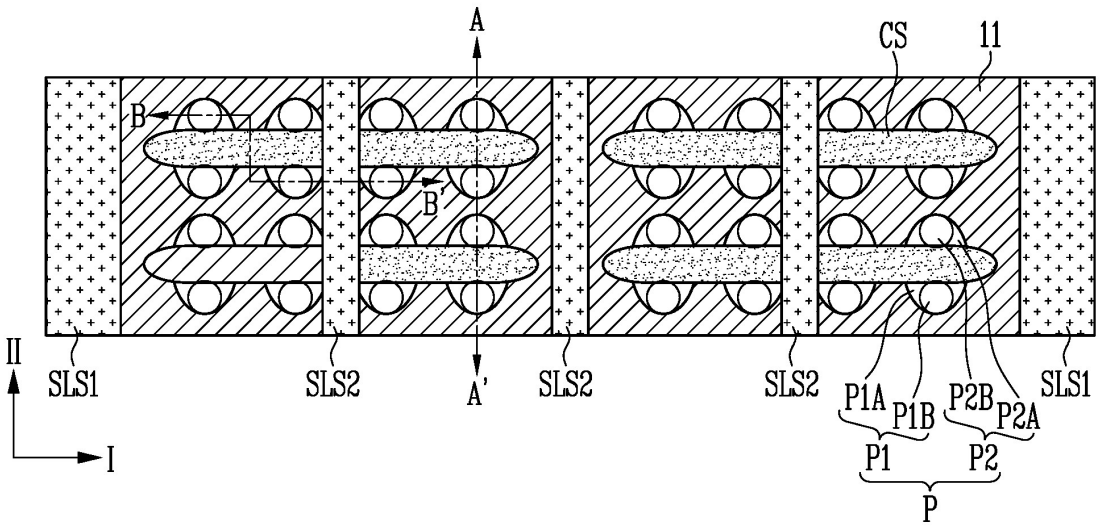


FIG. 4B

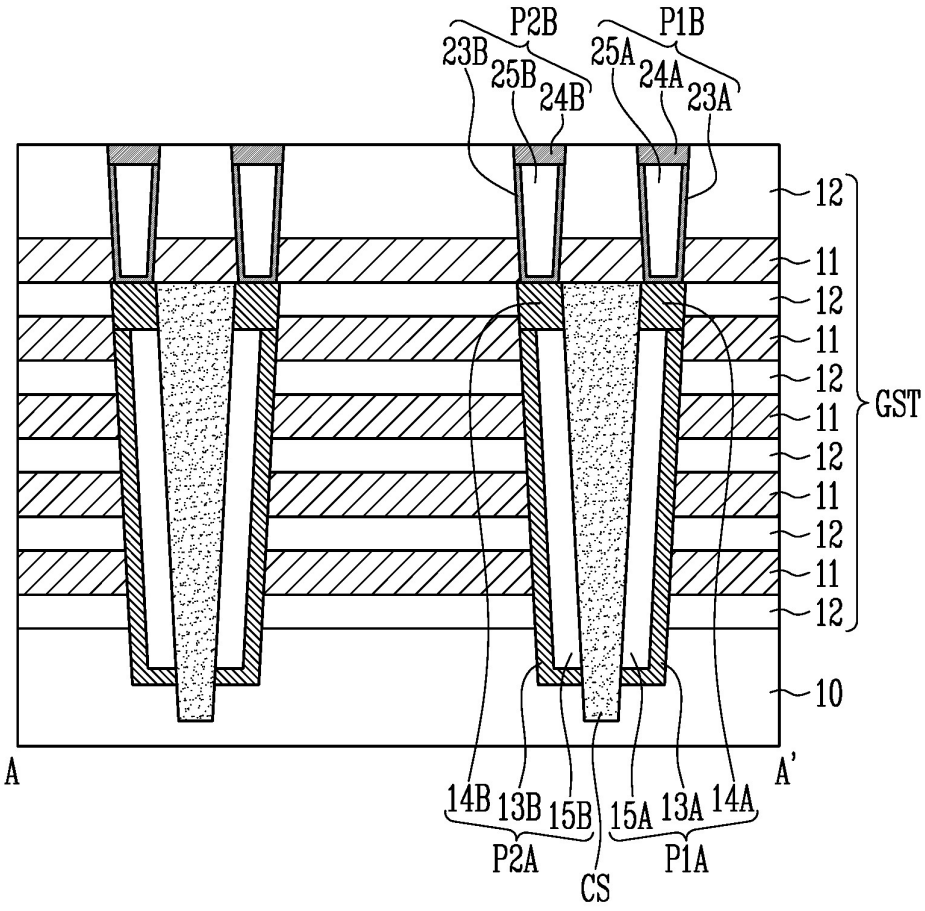

P2B
P1B
23B
25B
24B
25A
24A
23A
12
11
12
11
12
11
12
11
12
11
12
GST
10
A
A'
14B
13B
15B
15A
13A
14A
P2A
P1A
CS

FIG. 4C

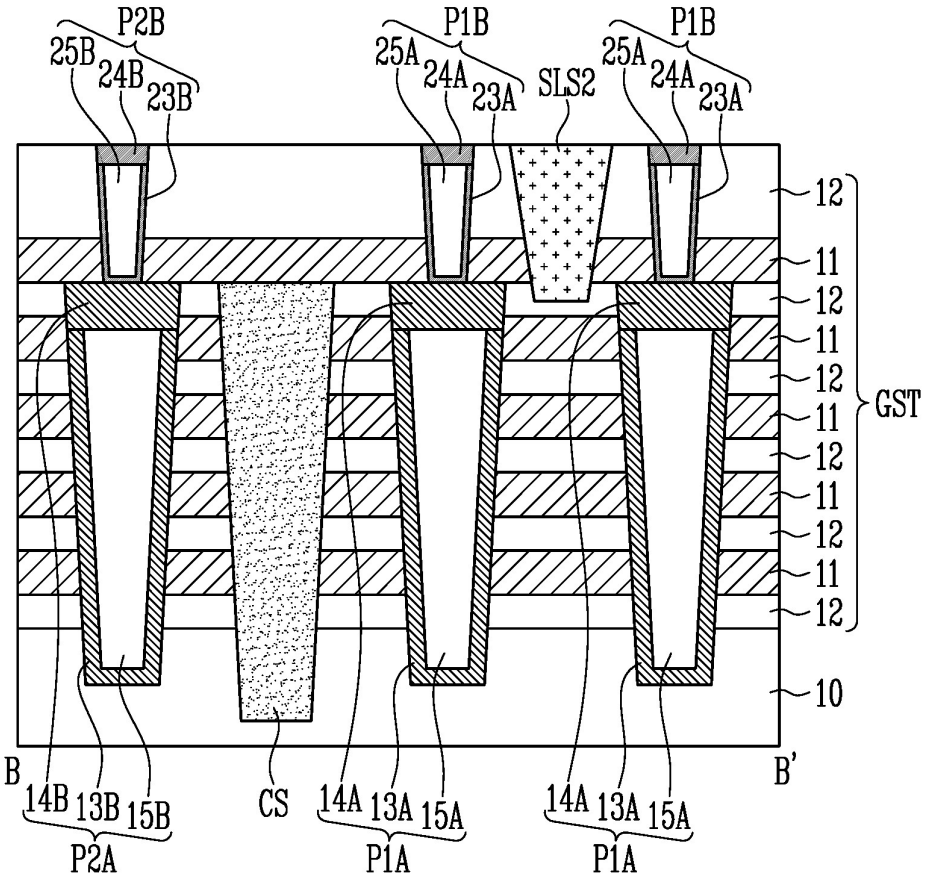

P2B
25B
24B
23B
P1B
25A
24A
23A
SLS2
P1B
25A
24A
23A
12
11
12
11
12
11
12
11
12
11
12
GST
10
B
14B
13B
15B
P2A
CS
14A
13A
15A
P1A
14A
13A
15A
P1A
B'

FIG. 4D

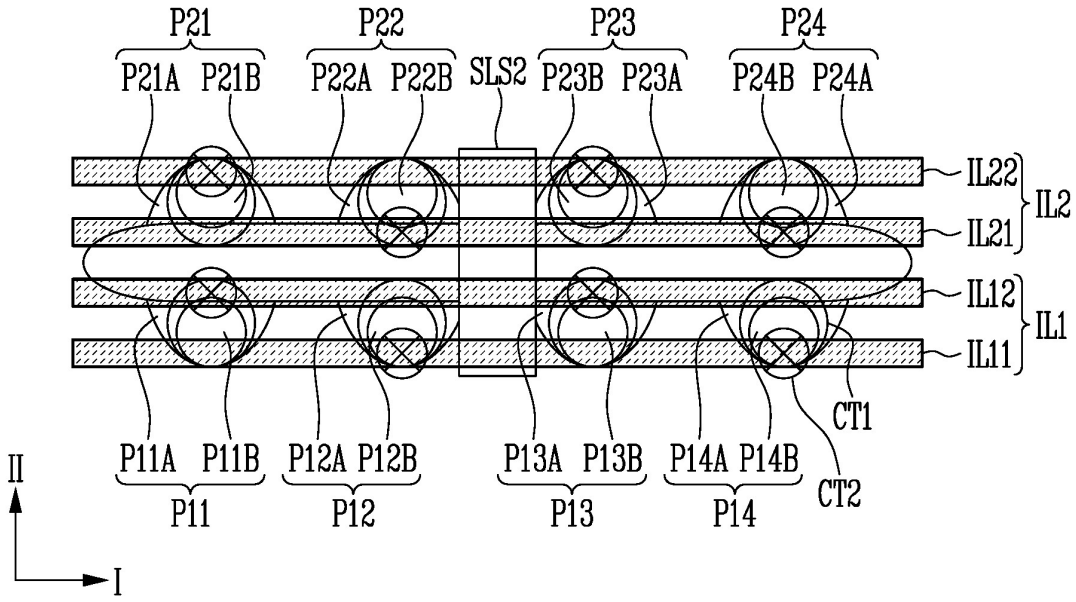

P21
P22
P23
P24
P21A P21B
P22A P22B
SLS2
P23B P23A
P24B P24A
IL22
IL21
IL2
IL12
IL11
IL1
CT1
CT2
P11A P11B
P12A P12B
P13A P13B
P14A P14B
P11
P12
P13
P14
II
I

FIG. 5A

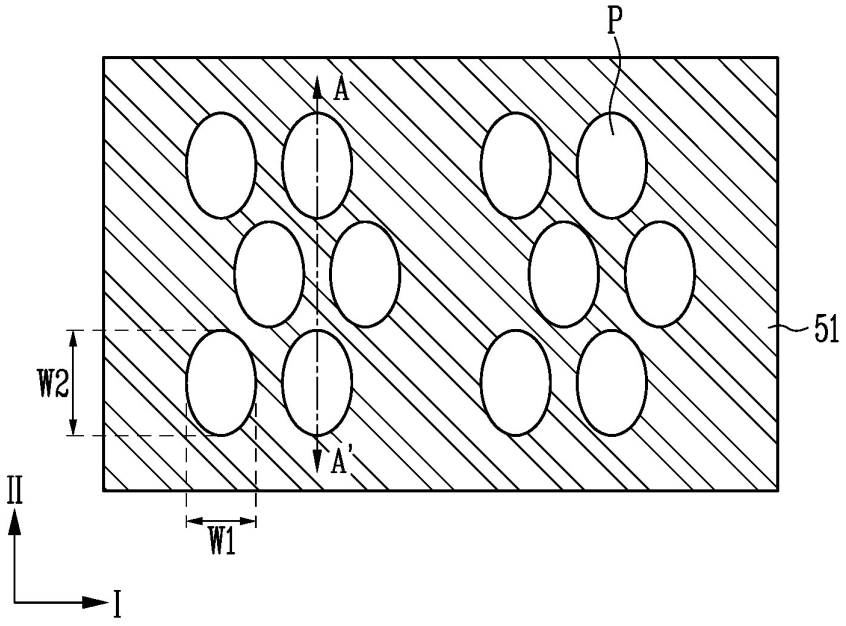

P
A
A'
51
W2
W1
II
I

FIG. 5B

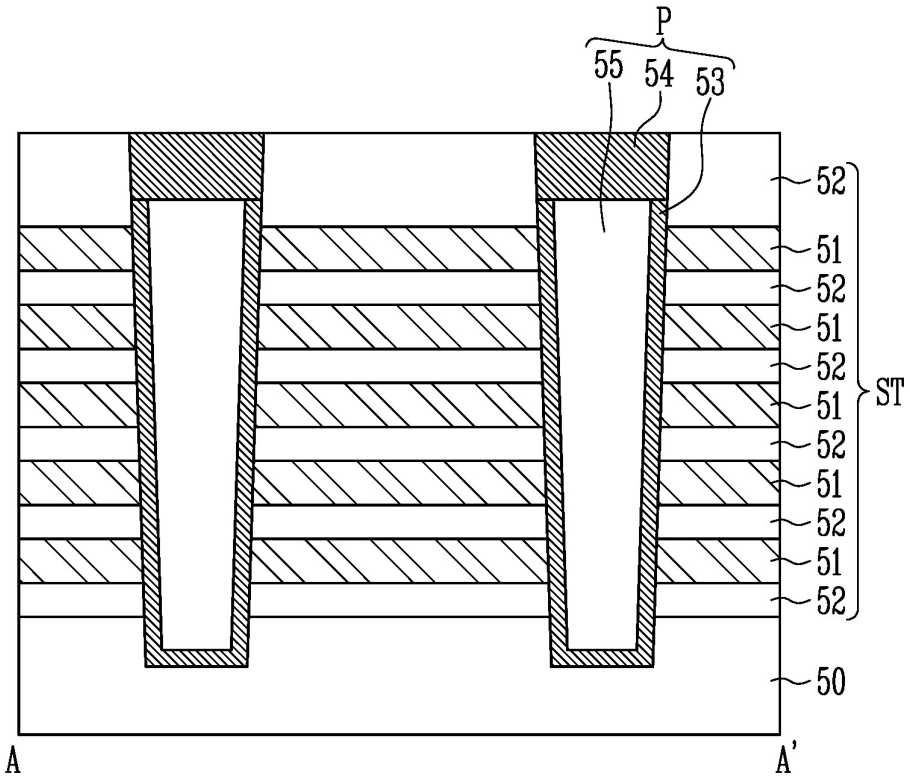


FIG. 6A

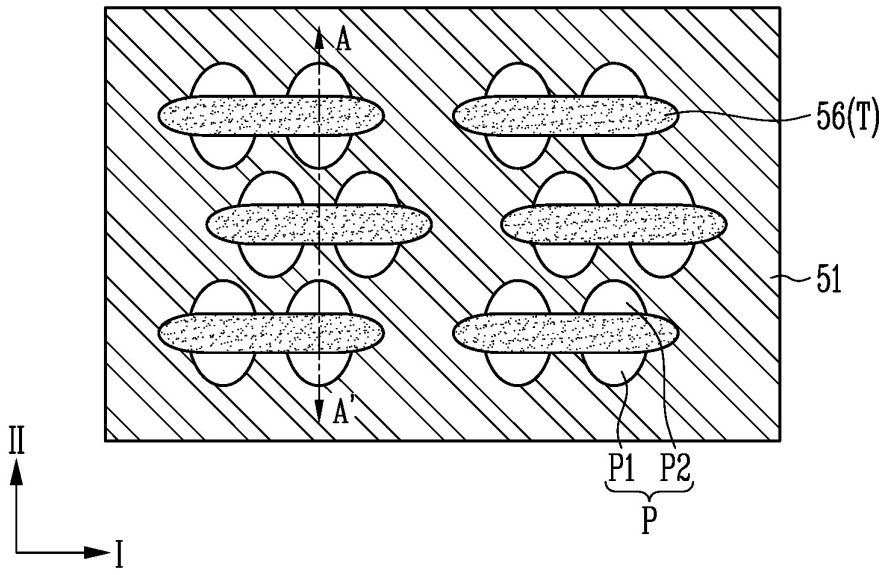


FIG. 6B

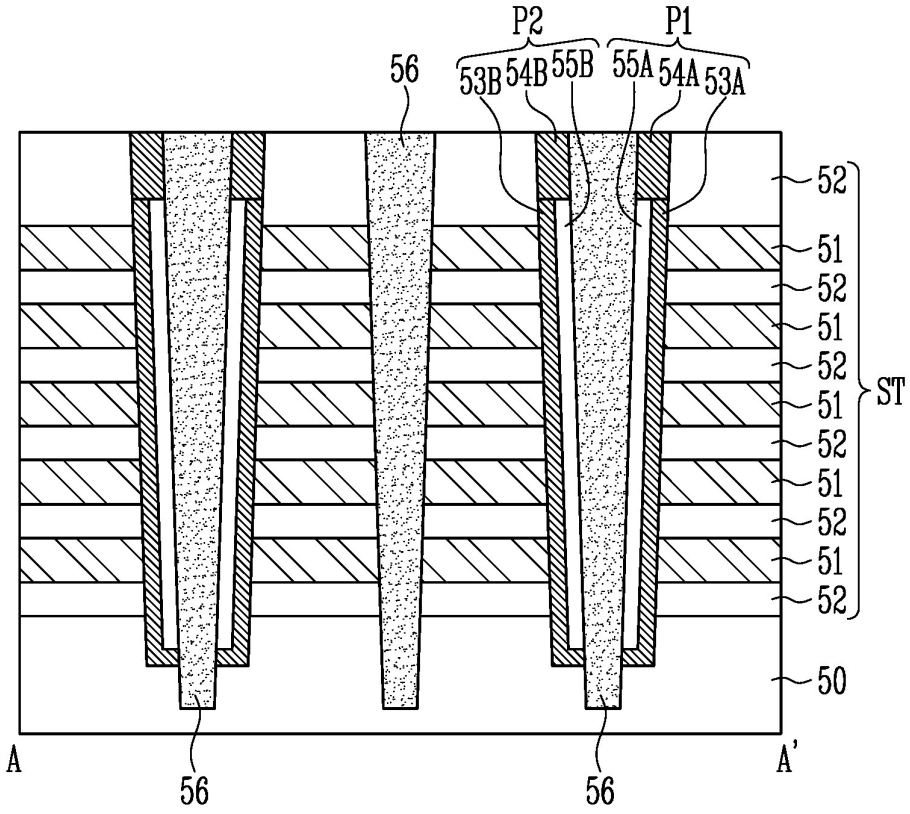

P2
P1
56
53B
54B
55B
55A
54A
53A
52
51
52
51
52
51
52
51
52
51
52
ST
50
A
A'
56
56

FIG. 7A

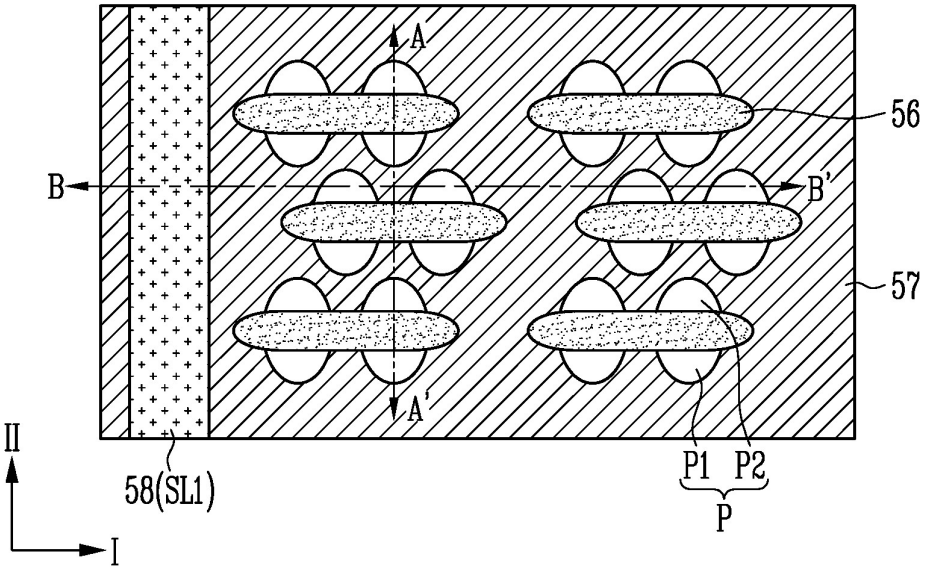


FIG. 7B

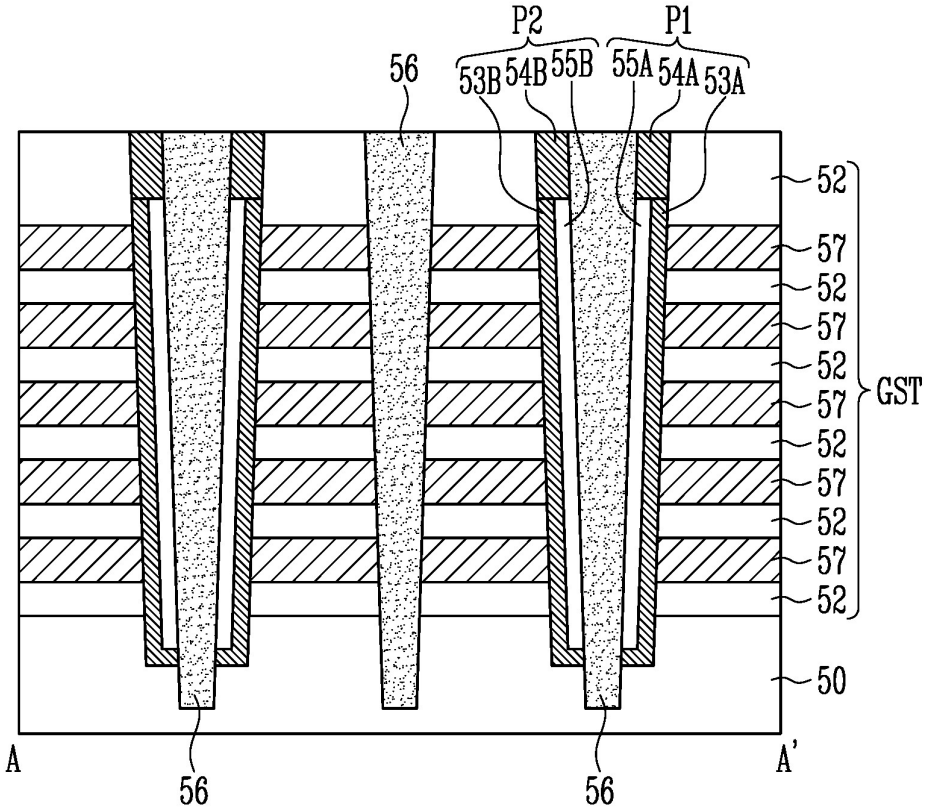

P2
P1
56
53B
54B
55B
55A
54A
53A
52
57
52
57
52
57
52
57
52
57
52
GST
50
A
A'
56
56

FIG. 7C

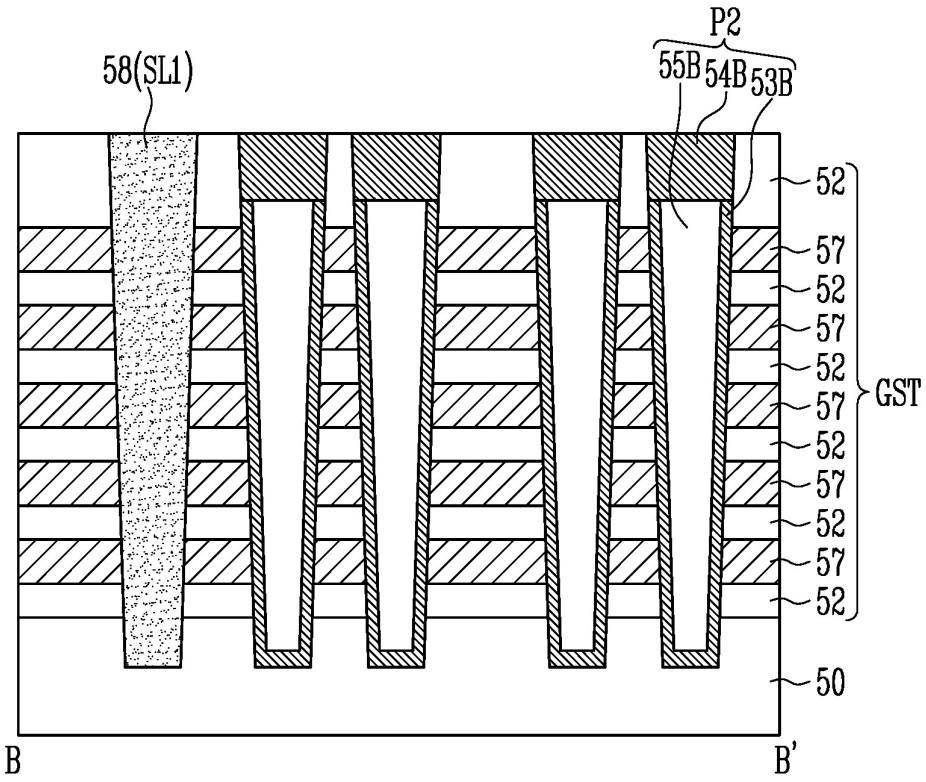


FIG. 8A

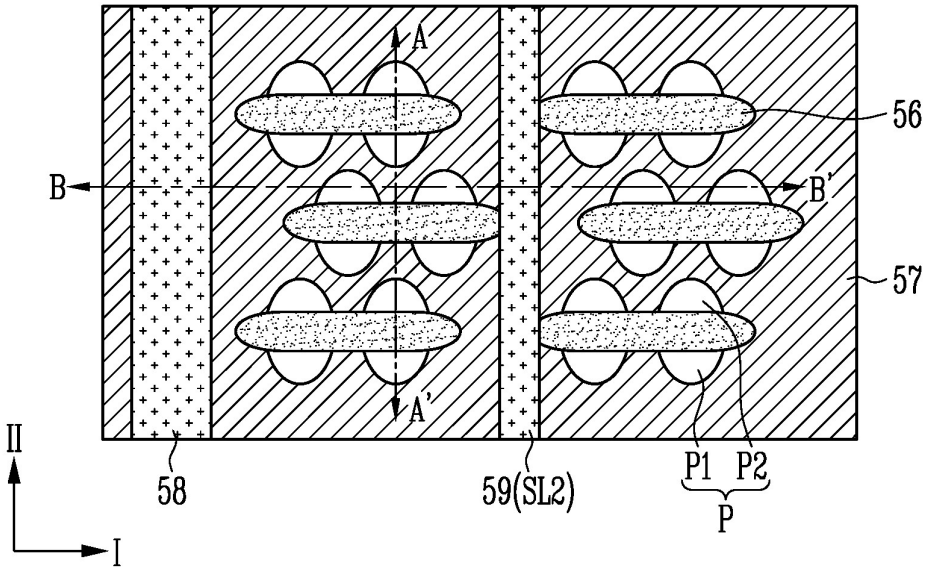


FIG. 8B

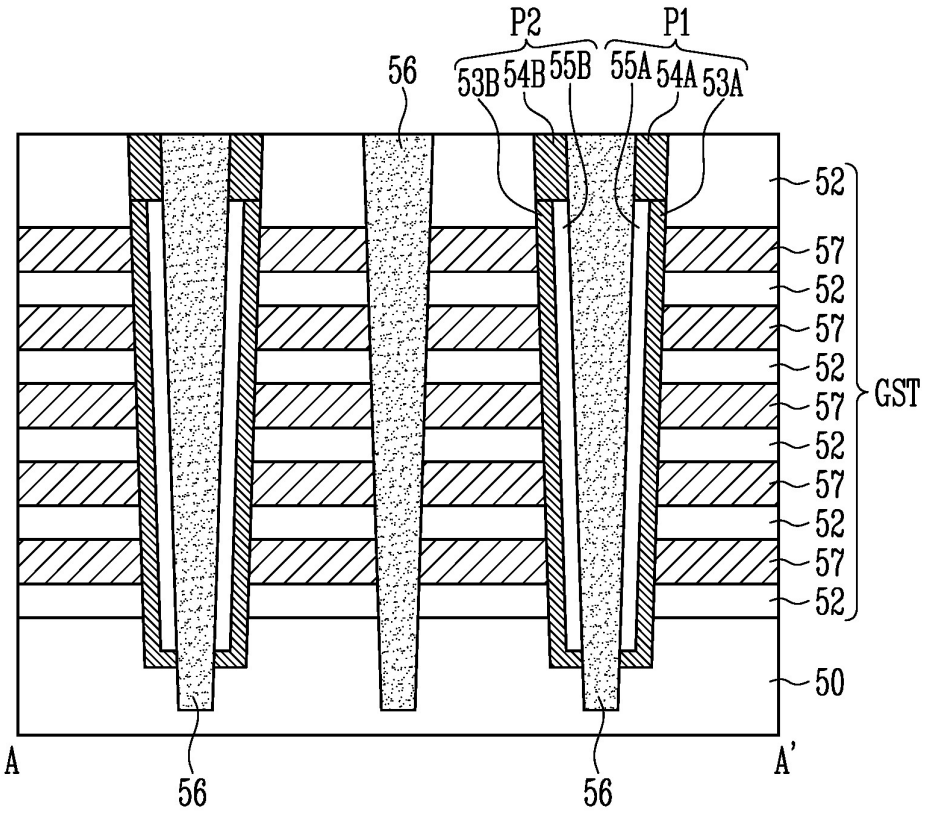

P2
P1
56
53B
54B
55B
55A
54A
53A
52
57
52
57
52
57
GST
52
57
52
57
52
50
A
56
56
A'

FIG. 8C

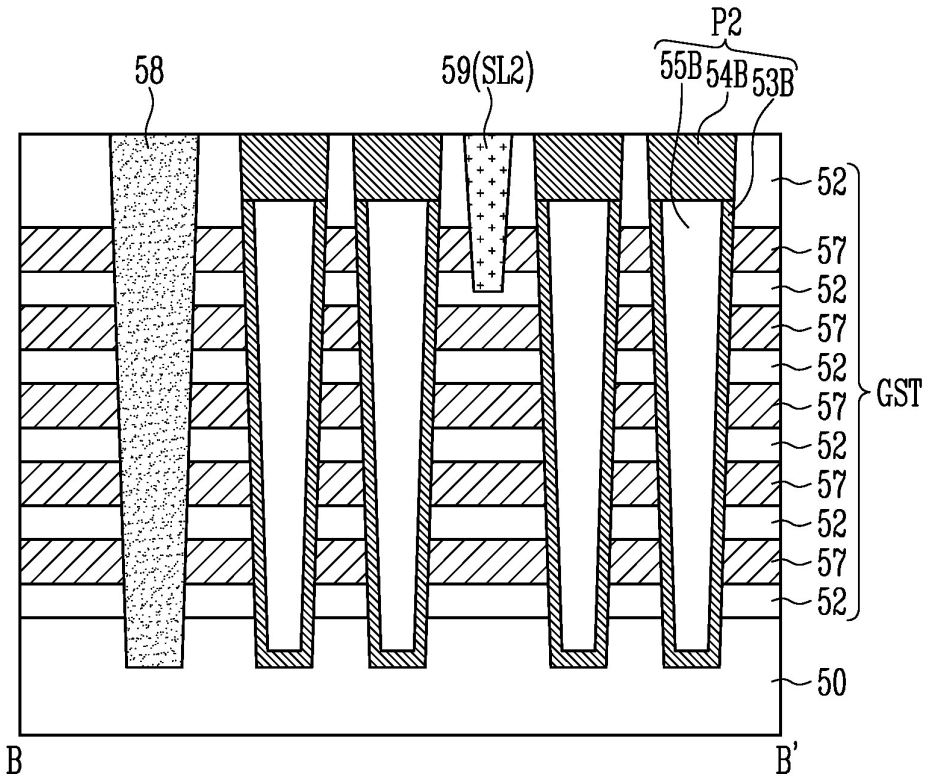


FIG. 9A

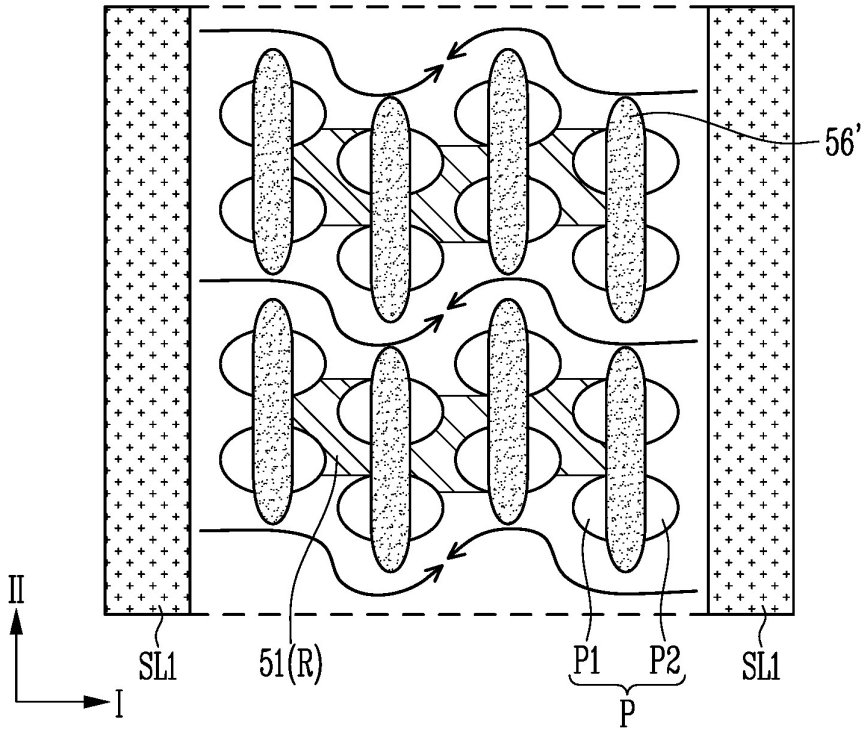


FIG. 9B

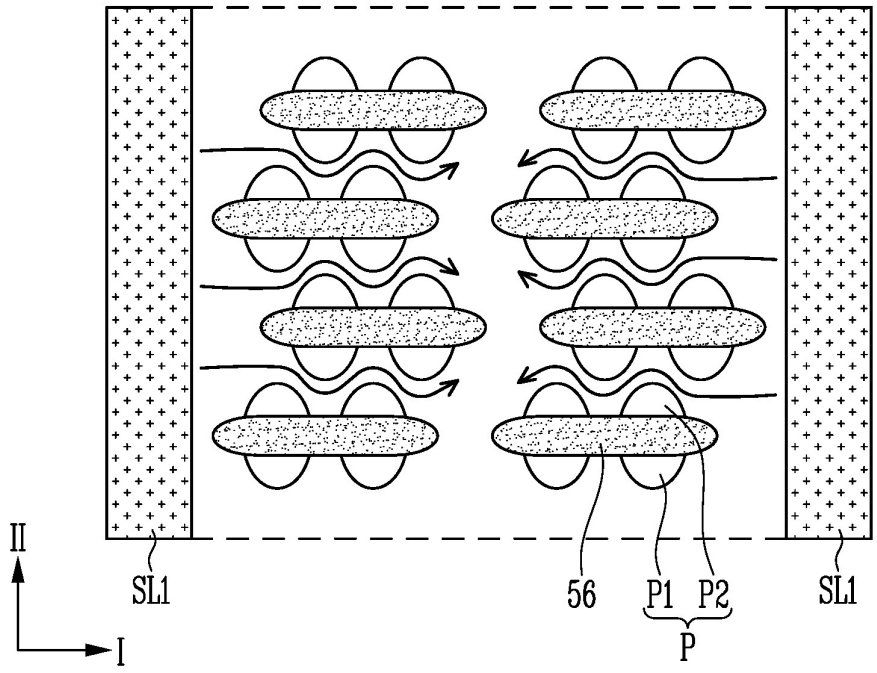


FIG. 10

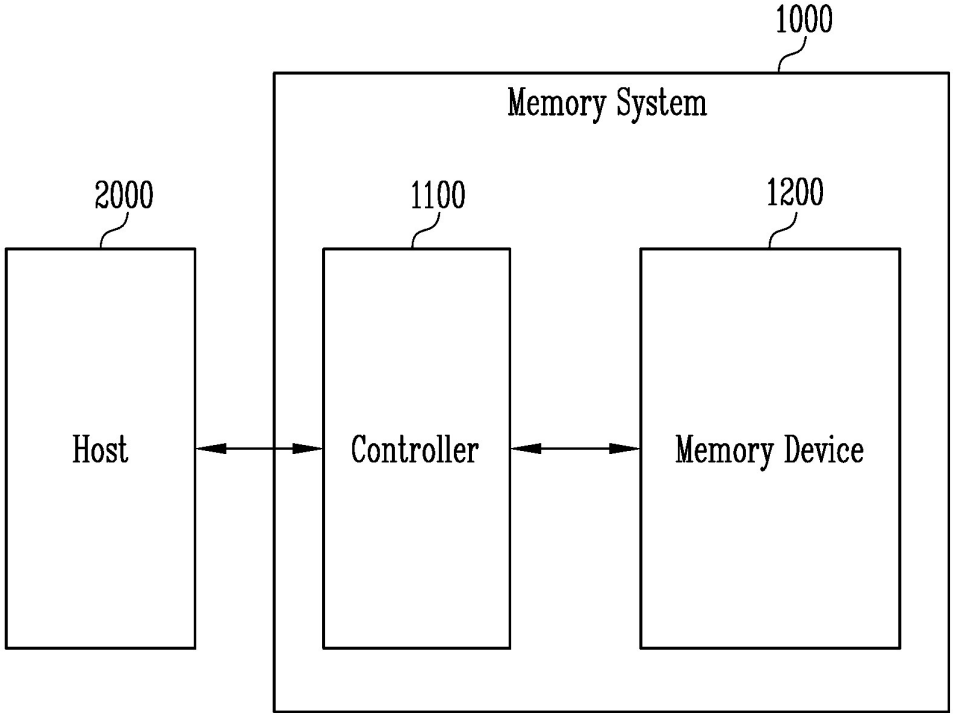

1000
Memory System
2000
1100
1200
Host
Controller
Memory Device

FIG. 11

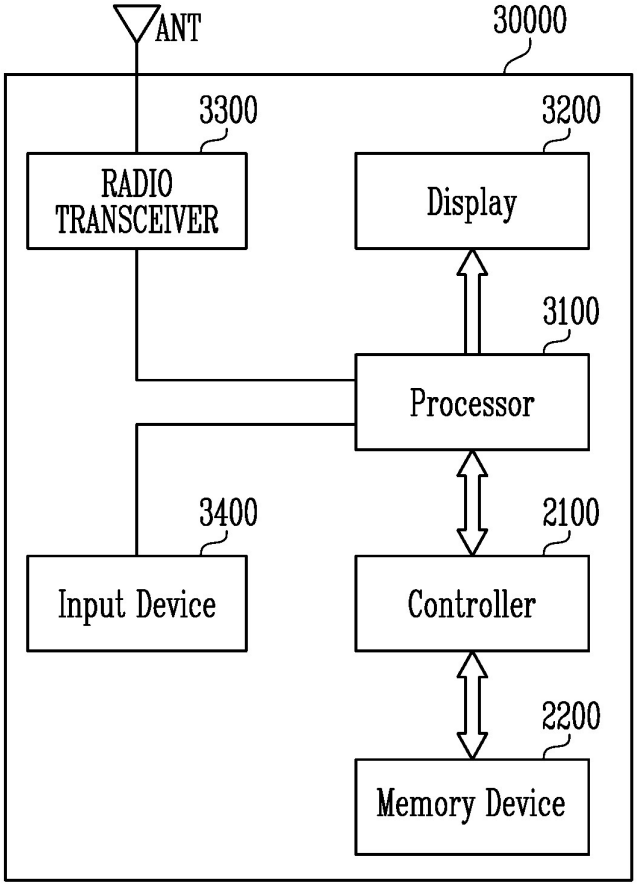

ANT
30000
3300
3200
RADIO TRANSCEIVER
Display
3100
Processor
3400
2100
Input Device
Controller
2200
Memory Device

FIG. 12

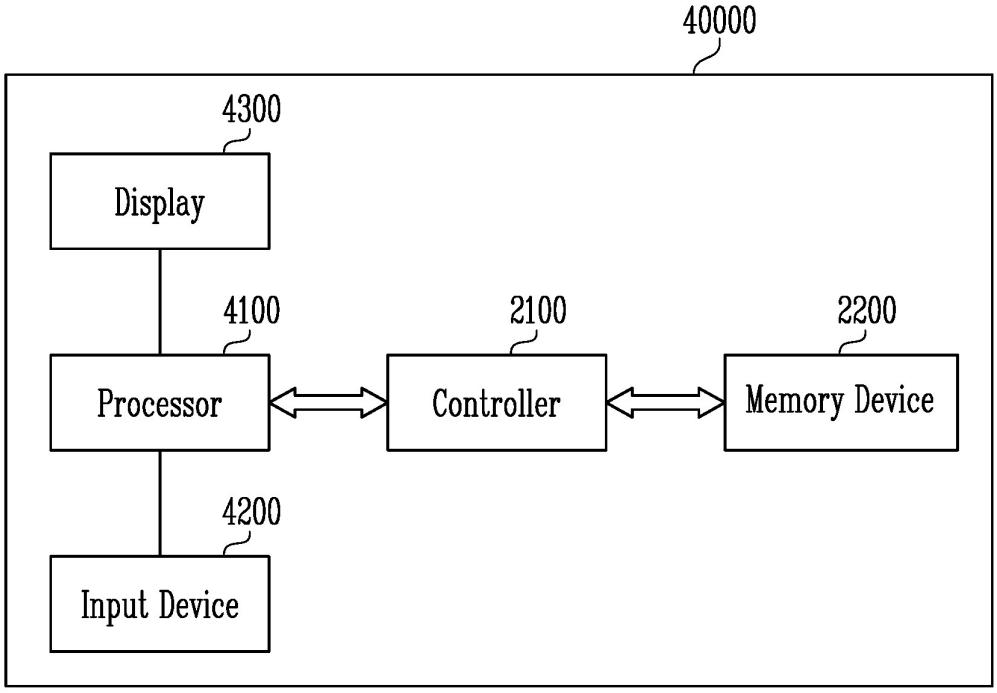

40000
4300
Display
4100
Processor
2100
Controller
2200
Memory Device
4200
Input Device

FIG. 13

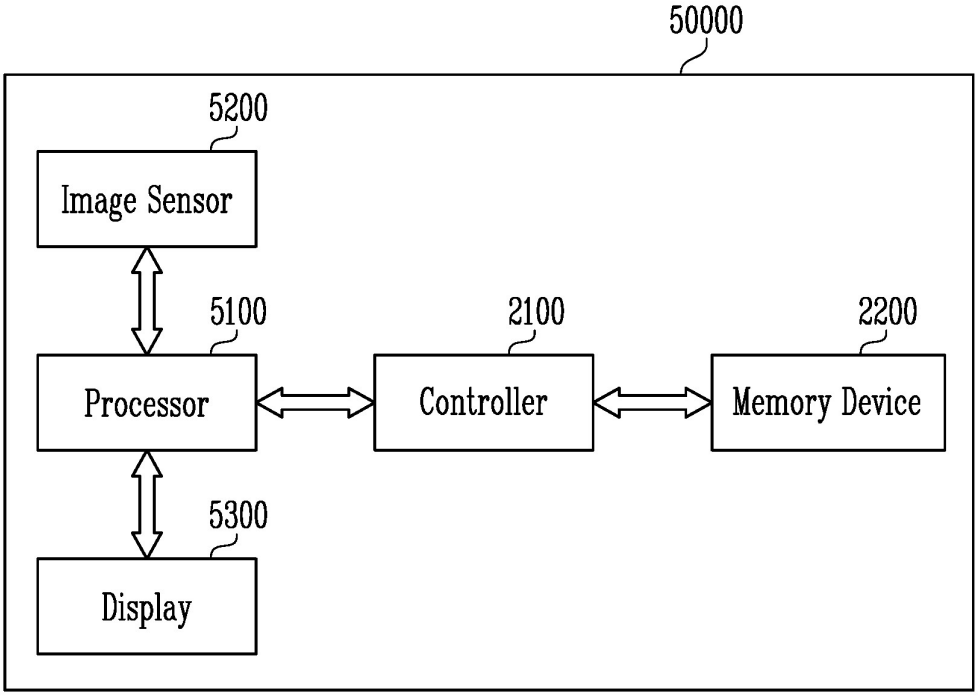
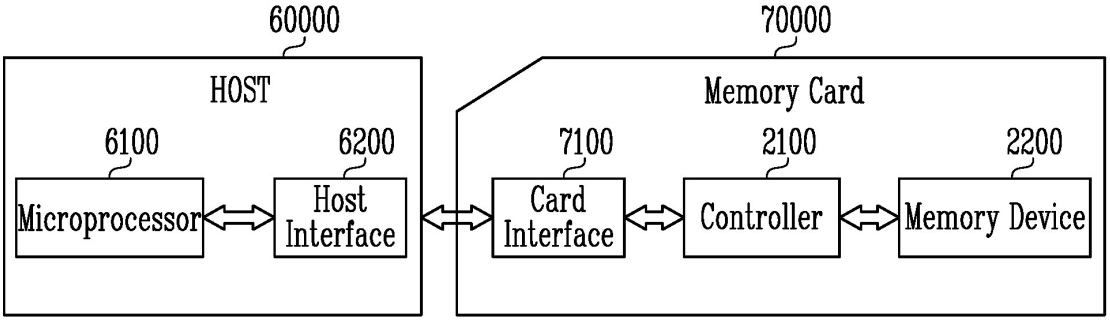

50000
5200
Image Sensor
5100
2100
2200
Processor
Controller
Memory Device
5300
Display

FIG. 14


60000
70000
HOST
Memory Card
6100
6200
7100
2100
2200
Microprocessor
Host Interface
Card Interface
Controller
Memory Device