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Abstract

Field-effect transistor, associated use and associated fabrication method

An explanation is given of a vertical field-effect transistor having a semiconductor layer (10), in which a doped channel region is arranged along a depression (72). A "buried" terminal region (18, 54) leads as far as a surface of the semiconductor layer (10). The field-effect transistor has outstanding electrical properties and is simple to fabricate.

(Figure 1C)

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