



- (51) International Patent Classification: Not classified
- (21) International Application Number: PCT/US2012/057081
- (22) International Filing Date: 25 September 2012 (25.09.2012)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 13/245,405 26 September 2011 (26.09.2011) US
- (71) Applicant: GLO AB [SE/SE]; Scheelevägen 17, Betahuset 6, IDEON SCIENCE PARK, S-223 70 Lund (SE).
- (72) Inventors: SVENSSON, Patrik; c/o GLO-USA, Inc., 1225 Bordeaux Drive, Sunnyvale, California 94089 (US). ROMANO, Linda; c/o GLO-USA, Inc., 1225 Bordeaux Drive, Sunnyvale, California 94089 (US). YI, Sungsoo; c/o GLO-USA, Inc., 1225 Bordeaux Drive, Sunnyvale, California 94089 (US). KRYLIOUK, Olga; c/o GLO-USA, Inc., 1225 Bordeaux Drive, Sunnyvale, California 94089 (US). CHANG, Ying-Lan; c/o GLO-USA, Inc., 1225 Bordeaux Drive, Sunnyvale, California 94089 (US).
- (74) Agents: RADOMSKY, Leon et al.; The Marbury Law Group, PLLC, 11800 Sunrise Valley Drive, 15th Floor, Reston, Virginia 20191 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ,

[Continued on next page]

- (54) Title: COALESCED NANOWIRE STRUCTURES WITH INTERSTITIAL VOIDS AND METHOD FOR MANUFACTURING THE SAME

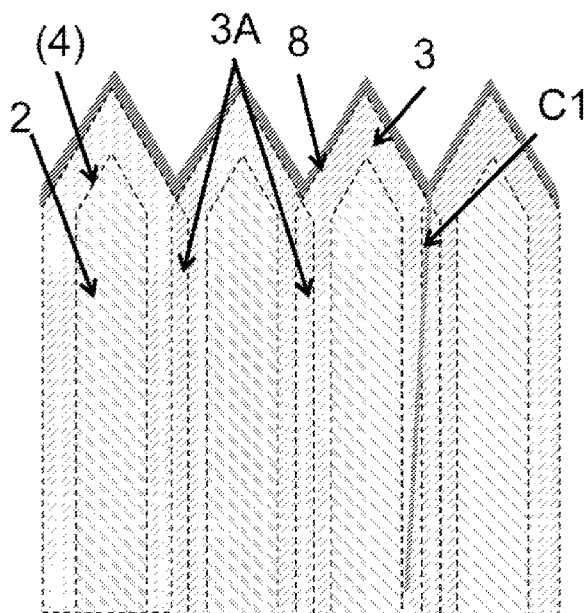


FIGURE 5A

- (57) Abstract: A semiconductor device, such as an LED, includes a plurality of first conductivity type semiconductor nanowire cores located over a support, a continuous second conductivity type semiconductor layer extending over and around the cores, a plurality of interstitial voids located in the second conductivity type semiconductor layer and extending between the cores, and first electrode layer that contacts the second conductivity type semiconductor layer.



TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- without international search report and to be republished upon receipt of that report (Rule 48.2(g))