CLAIMS

1. A word line driver comprising:

a substrate comprising an NMOS (N-Metal-Oxide-Semiconductor) area and a PMOS (P-Metal-Oxide-Semiconductor) area;

wherein the PMOS area comprises a plurality of first active areas extending along a first direction, and each first active area comprises a first channel area, and a first source area and a first drain area respectively located on opposite sides of the first channel area,

wherein the NMOS area and the PMOS area are arranged along a second direction, the NMOS area comprises a plurality of second active areas extending along the first direction, each second active area comprises a second channel area, and a second source area and a second drain area respectively located on opposite sides of the second channel area, and the each second active area further comprises a third channel area, and a third source area and a third drain area respectively located on opposite sides of the third channel area;

first gates, wherein the first gates are electrically connected to a main word line, a first gate, a first source area and a first drain area constitute a pull-up transistor, a first gate, a second source area and a second drain area constitute a pull-down transistor, the pull-up transistor and the pull-down transistor are electrically connected to a same sub word-line, and an extension direction of first gates corresponding to a first active area are inclined compared with the first direction;

a plurality of second gates, wherein each second gate covers a corresponding third channel area, and a second gate, a third source area and a third drain area constitute a holding transistor,

wherein, for a same holding transistor, a third drain area is electrically connected

to a second drain area of a pull-down transistor and a third source area is electrically connected to a second drain area of another pull-down transistor; and

first contact structures, wherein each first contact structure is electrically connected to a first source area or a first drain area, and extension directions of orthographic projections, of at least a partial number of the first contact structures, on a surface of the substrate are inclined compared with the first direction;

wherein an orthographic projection, of a first contact structure near an edge of a first active area, on the surface of substrate is triangular, and an extension direction of an orthographic projection, of a boundary of the first contact structure, on the substrate surface is inclined compared with the first direction, wherein the boundary towards a first gate.

2. The word line driver of claim 1, wherein each first gate extends along the second direction and covers a plurality of first channel areas and a plurality of second channel areas, and a first drain area of a pull-up transistor is electrically connected to a second drain area of a pull-down transistor, and is electrically connected to a corresponding sub word-line.

3. The word line driver of claim 1, wherein the PMOS area is located on one side of the NMOS area.

4. The word line driver of claim 1, wherein the NMOS area comprises a first NMOS area and a second NMOS area respectively located on opposite sides of the PMOS area.

5. The word line driver of claim 4, wherein the third channel area is located on one side of the second source area or second drain area along the second direction, and the third drain area of the holding transistor and a second drain area of a pull-down transistor are shared, and the third source area of the holding transistor and a second drain area of another pull-down transistor are shared.

6. A word line driver comprising:

a substrate comprising an NMOS (N-Metal-Oxide-Semiconductor) area and a PMOS (P-Metal-Oxide-Semiconductor) area;

wherein the PMOS area comprises a plurality of first active areas extending along a first direction, and each first active area comprises a first channel area, and a first source area and a first drain area respectively located on opposite sides of the first channel area,

wherein the NMOS area and the PMOS area are arranged along a second direction, the NMOS area comprises a plurality of second active areas extending along the first direction, each second active area comprises a second channel area, and a second source area and a second drain area respectively located on opposite sides of the second channel area, and the each second active area further comprises a third channel area, and a third source area and a third drain area respectively located on opposite sides of the third channel area;

first gates, wherein the first gates are electrically connected to a main word line, a first gate, a first source area and a first drain area constitute a pull-up transistor, a first gate, a second source area and a second drain area constitute a pull-down transistor, the pull-up transistor and the pull-down transistor are electrically connected to a same sub word-line, and an extension direction of first gates corresponding to a first active area are inclined compared with the first direction; and

a plurality of second gates, wherein each second gate covers a corresponding third channel area, and a second gate, a third source area and a third drain area constitute a holding transistor,

wherein, for a same holding transistor, a third drain area is electrically connected to a second drain area of a pull-down transistor and a third source area is electrically connected to a second drain area of another pull-down transistor,

wherein an extension direction of first gates corresponding to a second active area is inclined compared with the first direction;

wherein a length of a second active area is greater than a length of a first active area in the first direction, an inclined angle between an extending direction of the first gates corresponding to the second active area and the first direction is a first angle, an inclined angle between an extending direction of first gates corresponding to the first active area and the first direction is a second angle, and the first angle is less than the second angle.

7. The word line driver of claim 6, further comprising second contact structures, wherein each second contact structure is used to electrically connect to a second source area, a second drain area, and a third source area or third drain area, and an extension direction of an orthographic projection, of the second contact structure, on a surface of the substrate is inclined compared with the first direction.

8. The word line driver of claim 7, wherein a partial area of the orthographic projection, of the second contact structure, on the surface of the substrate is located outside of a second active area.

9. A word line driver comprising:

a substrate comprising an NMOS (N-Metal-Oxide-Semiconductor) area and a PMOS (P-Metal-Oxide-Semiconductor) area;

wherein the PMOS area comprises a plurality of first active areas extending along a first direction, and each first active area comprises a first channel area, and a first source area and a first drain area respectively located on opposite sides of the first channel area,

wherein the NMOS area and the PMOS area are arranged along a second direction, the NMOS area comprises a plurality of second active areas extending along the first direction, each second active area comprises a second channel area, and a second source area and a second drain area respectively located on opposite sides of the second channel area, and the each second active area further comprises a third channel area, and a third source area and a third drain area respectively located on opposite sides of the third channel area;

first gates, wherein the first gates are electrically connected to a main word line, a first gate, a first source area and a first drain area constitute a pull-up transistor, a first gate, a second source area and a second drain area constitute a pull-down transistor, the pull-up transistor and the pull-down transistor are electrically connected to a same sub word-line, and an extension direction of first gates corresponding to a first active area are inclined compared with the first direction;

a plurality of second gates, wherein each second gate covers a corresponding third channel area, and a second gate, a third source area and a third drain area constitute a holding transistor,

wherein, for a same holding transistor, a third drain area is electrically connected to a second drain area of a pull-down transistor and a third source area is electrically connected to a second drain area of another pull-down transistor; and

third contact structures, wherein each third contact structure is used to electrically

connect to adjacent second active areas.

10. The word line driver of claim 1, wherein a second drain area of a pull-down transistor corresponding a first gate and a third drain area of the holding transistor are shared, and a second drain area of another pull-down transistor corresponding the same first gate and a third source area of the same holding transistor are shared.

11. The word line driver of claim 1, wherein a second drain area of a pull-down transistor corresponding to a first gate and a third drain area of the holding transistor are shared, and a second drain area of a pull-down transistor corresponding to another first gate and a third source area of the same holding transistor are shared.

12. The word line driver of claim 11, wherein a second gate is located between adjacent first gates.

13. A word line driver comprising:

a substrate comprising an NMOS (N-Metal-Oxide-Semiconductor) area and a PMOS (P-Metal-Oxide-Semiconductor) area;

wherein the PMOS area comprises a plurality of first active areas extending along a first direction, and each first active area comprises a first channel area, and a first source area and a first drain area respectively located on opposite sides of the first channel area,

wherein the NMOS area and the PMOS area are arranged along a second direction, the NMOS area comprises a plurality of second active areas extending along

the first direction, each second active area comprises a second channel area, and a second source area and a second drain area respectively located on opposite sides of the second channel area, and the each second active area further comprises a third channel area, and a third source area and a third drain area respectively located on opposite sides of the third channel area;

first gates, wherein the first gates are electrically connected to a main word line, a first gate, a first source area and a first drain area constitute a pull-up transistor, a first gate, a second source area and a second drain area constitute a pull-down transistor, the pull-up transistor and the pull-down transistor are electrically connected to a same sub word-line, and an extension direction of first gates corresponding to a first active area are inclined compared with the first direction;

a plurality of second gates, wherein each second gate covers a corresponding third channel area, and a second gate, a third source area and a third drain area constitute a holding transistor,

wherein, for a same holding transistor, a third drain area is electrically connected to a second drain area of a pull-down transistor and a third source area is electrically connected to a second drain area of another pull-down transistor; and

wherein the holding transistor comprises: a first transistor and a second transistor, two pull-down transistors electrically connected to a same first transistor share a first gate, for a same second transistor, a third drain area is electrically connected to a second drain area of a pull-down transistor and a third source area is electrically connected to a second drain area of another pull-down transistor, and two pull-down transistors electrically connected to a same second transistor correspond to two first gates.

14. The word line driver of claim 13, wherein the NMOS area comprises:

a first NMOS area and a second NMOS area that are respectively located at

opposite sides of the PMOS area,

wherein the first transistor is located in the first NMOS area, the second transistor is located in the second NMOS area, a part number of pull-down transistors are located in the first NMOS area, and a remaining number of the pull-down transistors are located in the second NMOS area.

15. The word line driver of claim 1, wherein each first gate comprises:

at least two extension portions arranged at intervals along the first direction, wherein each extension portion covers a plurality of first channel areas and a plurality of second channel areas, and is inclined compared with the first direction; and

a connecting portion, wherein the connecting portion connects extension portions arranged adjacent to each other in the first direction.

16. The word line driver of claim 1, wherein a first gate covers $4 \times N$ first channel areas and $4 \times N$ second channel areas, and pull-up transistors and pull-down transistors composed of each first gate are electrically connected to $2 \times N$ holding transistors, wherein N is a positive integer greater than or equal to 1.

17. A memory device comprising:

a memory cell array comprising a plurality of memory cells connected to a plurality of sub word-lines and a plurality of bit lines; and

a word line driver of any one of claims 1-16.