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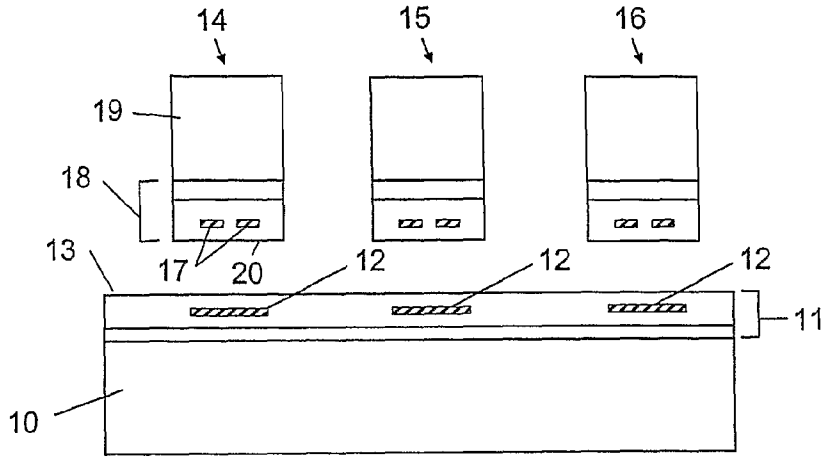
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(54) **Title:** 3D IC METHOD AND DEVICE



(57) **Abstract:** A method of three-dimensionally integrating elements such as singulated die or wafers and an integrated structure having connected elements such as singulated dies or wafers. Either or both of the die and wafer may have semiconductor devices formed therein. A first element having a first contact structure is bonded to a second element having a second contact structure. First and second contact structures can be exposed at bonding and electrically interconnected as a result of the bonding. A via may be etched and filled after bonding to expose and form an electrical interconnect to interconnected first and second contact structures and provide electrical access to this interconnect from a surface. Alternatively, first and/or second contact structures are not exposed at bonding, and a via is etched and filled after bonding to electrically interconnect first and second contact structures and provide electrical access to interconnected first and second contact structure to a surface. Also, a device may be formed in a first substrate, the device being disposed in a device region of the first substrate and having a first contact structure. A via may be etched, or etched and filled, through the device region and into the first substrate before bonding and the first substrate thinned to expose the via, or filled via after bonding.

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