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DYNAMIC BUS ARBITRATION

Abstract

Apparatus and method for optimizing bus arbitration during direct memory access (DMA) data transfers across a nondedicated bus between a memory and/or a plurality of external devices each master having an arbitration priority. At least two nonoverlapping clocks are provided per transfer cycle and there is at least one transfer cycle per arbitration cycle. Arbitration priority requests are transmitted from each external device to an arbitration bus only at the rise of the first clock. At the end of the last clock, the priority code of the external device having the highest priority is determined to designate the external device which is to become bus master. Addresses and data are transferred between the designated bus master and the memory or another of the external devices via the nondedicated bus during the next cycle after a then active bus master relinquishes control. The priorities of the external devices can be changed dynamically.

Arbitration cycles are pipelined in such manner that there is no loss of address or data transfer cycles. The then active bus master may extend the number of cycles during which it communicates with one or more external devices. A device designated as next in line as bus master may be pre-empted under a certain condition.

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